

1. Overview

1.1 Features

The M16C Family offers a robust platform of 32-/16-bit CISC microcomputers (MCUs) featuring high ROM code efficiency, extensive EMI/EMS noise immunity, ultra-low power consumption, high-speed processing in actual applications, and numerous and varied integrated peripherals. Extensive device scalability from low- to high-end, featuring a single architecture as well as compatible pin assignments and peripheral functions, provides support for a vast range of application fields.

The R32C/100 Series is a high-end microcontroller series in the M16C Family. With a 4-Gbyte memory space, it achieves maximum code efficiency and high-speed processing with 32-bit CISC architecture, multiplier, multiply-accumulate unit, and floating point unit. The selection from the broadest choice of on-chip peripheral devices — UART, CRC, DMAC, A/D and D/A converters, timers, I²C, and WDT enables to minimize external components.

The R32C/100 Series, in particular, provides the R32C/118A Group as a standard product. This product, provided as a 144/176-pin plastic molded LQFP package, configures 11 channels of serial interface, one channel of multi-master I²C-bus interface, and two channels of CAN module.

1.1.1 Applications

Car audio, audio, printer, office/industrial equipment, etc.

1.1.2 Performance Overview

Table 1.1 to Table 1.4 show the performance overview of the R32C/118A Group.

Table 1.1 R32C/118A Group Performance for the 176 pin-Package (1/2)

| Unit | Function | Performance |
|------------------------|--------------------------|---|
| CPU | Central processing unit | R32C/100 Series CPU Core <ul style="list-style-type: none"> • Basic instructions: 108 • Minimum instruction execution time: 15.625 ns ($f(\text{CPU}) = 64 \text{ MHz}$) • Multiplier: 32-bit \times 32-bit \rightarrow 64-bit • Multiply-accumulate unit: 32-bit \times 32-bit + 64-bit \rightarrow 64-bit • IEEE-754 floating point standard: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional ⁽¹⁾) |
| Memory | | Flash memory: 512 Kbytes to 1 Mbyte RAM: 96 Kbytes Data flash: 4 Kbytes \times 2 blocks Refer to Table 1.5 for memory size of each product group |
| Voltage Detector | Low voltage detector | Optional ⁽¹⁾ Low voltage detection interrupt |
| Clock | Clock generator | <ul style="list-style-type: none"> • 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/re-oscillation detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode |
| External Bus Expansion | Bus and memory expansion | <ul style="list-style-type: none"> • Address space: 4 Gbytes (of which up to 64 Mbytes is user accessible) • External bus Interface: Support for wait-state insertion, 4 chip select outputs • Bus format: Separate bus/Multiplexed bus selectable, data bus width selectable (8/16/32 bits) |
| Interrupts | | Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}} \times 9$, key input $\times 4$ Interrupt priority levels: 7 levels |
| Watchdog Timer | | 15 bits \times 1 (selectable input frequency from prescaler output) • Automatic timer start function is available |
| DMA | DMAC | 4 channels <ul style="list-style-type: none"> • Cycle-steal transfer mode • Request sources: 61 • 2 transfer modes: Single transfer, repeat transfer |
| | DMAC II | <ul style="list-style-type: none"> • Can be activated by any peripheral interrupt source • 3 transfer functions: Immediate data transfer, calculation transfer, chained transfer |
| I/O Ports | Programmable I/O ports | <ul style="list-style-type: none"> • 2 input-only ports • 156 CMOS inputs/outputs <ul style="list-style-type: none"> • 52 ports are 5 V tolerant • A pull-up resistor is selectable for every 4 input ports (except 5 V tolerant inputs) |

Note:

1. Please contact a Renesas Electronics sales office to use the optional feature.

Table 1.2 R32C/118A Group Performance for the 176-pin Package (2/2)

| Unit | Function | Performance |
|---|---------------------------------|--|
| Timer | Timer A | 16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 |
| | Timer B | 16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode |
| | Three-phase motor control timer | Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer |
| Serial Interface | UART0 to UART10 | Asynchronous/synchronous serial interface × 11 channels <ul style="list-style-type: none"> • I²C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (optional ⁽¹⁾) (UART0 to UART6) |
| A/D Converter | | 10-bit resolution × 34 channels Sample and hold functionality integrated Self test/Open-circuit detection assist |
| D/A Converter | | 8-bit resolution × 2 |
| CRC Calculator | | CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) |
| X-Y Converter | | 16 bits × 16 bits |
| Intelligent I/O | | Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 24 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional ⁽¹⁾) |
| Multi-master I ² C-bus Interface | | 1 channel |
| CAN Module | | 2 channels CAN functionality compliant with ISO11898-1 32 mailboxes |
| Flash Memory | | Programming and erasure supply voltage: VCC = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Suspend/resume function available Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming |
| Operating Frequency/Supply Voltage | | 64 MHz/VCC = 3.0 to 5.5 V |
| Operating Temperature | | -20°C to 85°C (N version) -40°C to 85°C (D version) -40°C to 85°C (P version) |
| Current Consumption | | 45 mA (VCC = 5.0 V, f(CPU) = 64 MHz) 8 μA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode) |
| Package | | 176-pin plastic molded LQFP (PLQP0176KB-A) |

Note:

1. Please contact a Renesas Electronics sales office to use the optional feature.

Table 1.3 R32C/118A Group Performance for the 144-pin Package (1/2)

| Unit | Function | Performance |
|------------------------|--------------------------|---|
| CPU | Central processing unit | R32C/100 Series CPU Core <ul style="list-style-type: none"> • Basic instructions: 108 • Minimum instruction execution time: 15.625 ns ($f(\text{CPU}) = 64 \text{ MHz}$) • Multiplier: 32-bit \times 32-bit \rightarrow 64-bit • Multiply-accumulate unit: 32-bit \times 32-bit + 64-bit \rightarrow 64-bit • IEEE-754 floating point standard: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional ⁽¹⁾) |
| Memory | | Flash memory: 512 Kbytes to 1 Mbyte RAM: 96 Kbytes Data flash: 4 Kbytes \times 2 blocks Refer to Table 1.5 for memory size of each product group |
| Voltage Detector | Low voltage detector | Optional ⁽¹⁾ Low voltage detection interrupt |
| Clock | Clock generator | <ul style="list-style-type: none"> • 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/re-oscillation detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode |
| External Bus Expansion | Bus and memory expansion | <ul style="list-style-type: none"> • Address space: 4 Gbytes (of which up to 64 Mbytes is user accessible) • External bus Interface: Support for wait-state insertion, 4 chip select outputs • Bus format: Separate bus/Multiplexed bus selectable, data bus width selectable (8/16/32 bits) |
| Interrupts | | Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}} \times 9$, key input $\times 4$ Interrupt priority levels: 7 levels |
| Watchdog Timer | | 15 bits \times 1 (selectable input frequency from prescaler output) Automatic timer start function is available |
| DMA | DMAC | 4 channels <ul style="list-style-type: none"> • Cycle-steal transfer mode • Request sources: 61 • 2 transfer modes: Single transfer, repeat transfer |
| | DMAC II | <ul style="list-style-type: none"> • Can be activated by any peripheral interrupt source • 3 transfer functions: Immediate data transfer, calculation transfer, chained transfer |
| I/O Ports | Programmable I/O ports | <ul style="list-style-type: none"> • 2 input-only ports • 124 CMOS inputs/outputs <ul style="list-style-type: none"> • 40 ports are 5 V tolerant • A pull-up resistor is selectable for every 4 input ports (except 5 V tolerant inputs) |

Note:

1. Please contact a Renesas Electronics sales office to use the optional feature.

Table 1.4 R32C/118A Group Performance for the 144-pin Package (2/2)

| Unit | Function | Performance |
|---|---------------------------------|--|
| Timer | Timer A | 16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 |
| | Timer B | 16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode |
| | Three-phase motor control timer | Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer |
| Serial Interface | UART0 to UART10 | Asynchronous/synchronous serial interface × 11 channels <ul style="list-style-type: none"> • I²C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (optional ⁽¹⁾) (UART0 to UART6) |
| A/D Converter | | 10-bit resolution × 34 channels Sample and hold functionality integrated Self test/Open-circuit detection assist |
| D/A Converter | | 8-bit resolution × 2 |
| CRC Calculator | | CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) |
| X-Y Converter | | 16 bits × 16 bits |
| Intelligent I/O | | Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 24 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional ⁽¹⁾) |
| Multi-master I ² C-bus Interface | | 1 channel |
| CAN Module | | 2 channels CAN functionality compliant with ISO11898-1 32 mailboxes |
| Flash Memory | | Programming and erasure supply voltage: VCC = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Suspend/resume function available Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming |
| Operating Frequency/Supply Voltage | | 64 MHz/VCC = 3.0 to 5.5 V |
| Operating Temperature | | -20°C to 85°C (N version) -40°C to 85°C (D version) -40°C to 85°C (P version) |
| Current Consumption | | 45 mA (VCC = 5.0 V, f(CPU) = 64 MHz) 8 μA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode) |
| Package | | 144-pin plastic molded LQFP (PLQP0144KA-A) |

Note:

1. Please contact a Renesas Electronics sales office to use the optional feature.

1.2 Product Information

Table 1.5 lists the product information and Figure 1.1 shows the details of the part number.

Table 1.5 R32C/118A Group Product List

As of July, 2010

| Part Number | Package Code (1) | ROM Capacity (2) | RAM Capacity | Remarks |
|------------------|------------------|--------------------------|--------------|---------------------------|
| R5F6418JANFE (P) | PLQP0176KB-A | 512 Kbytes + 8 Kbytes | 96 Kbytes | -20°C to 85°C (N version) |
| R5F6418JADFE (P) | | | | -40°C to 85°C (D version) |
| R5F6418JAPFE (P) | | | | -40°C to 85°C (P version) |
| R5F6418JANFD (P) | PLQP0144KA-A | 512 Kbytes + 8 Kbytes | 96 Kbytes | -20°C to 85°C (N version) |
| R5F6418JADFD (P) | | | | -40°C to 85°C (D version) |
| R5F6418JAPFD (P) | | | | -40°C to 85°C (P version) |
| R5F6418KANFE (P) | PLQP0176KB-A | 640 Kbytes + 8 Kbytes | 96 Kbytes | -20°C to 85°C (N version) |
| R5F6418KADFE (P) | | | | -40°C to 85°C (D version) |
| R5F6418KAPFE (P) | | | | -40°C to 85°C (P version) |
| R5F6418KANFD (P) | PLQP0144KA-A | 640 Kbytes + 8 Kbytes | 96 Kbytes | -20°C to 85°C (N version) |
| R5F6418KADFD (P) | | | | -40°C to 85°C (D version) |
| R5F6418KAPFD (P) | | | | -40°C to 85°C (P version) |
| R5F6418LANFE (P) | PLQP0176KB-A | 768 Kbytes + 8 Kbytes | 96 Kbytes | -20°C to 85°C (N version) |
| R5F6418LADFE (D) | | | | -40°C to 85°C (D version) |
| R5F6418LAPFE (D) | | | | -40°C to 85°C (P version) |
| R5F6418LANFD (P) | PLQP0144KA-A | 768 Kbytes + 8 Kbytes | 96 Kbytes | -20°C to 85°C (N version) |
| R5F6418LADFD (D) | | | | -40°C to 85°C (D version) |
| R5F6418LAPFD (D) | | | | -40°C to 85°C (P version) |
| R5F6418MANFE (P) | PLQP0176KB-A | 1 Mbyte + 8 Kbytes | 96 Kbytes | -20°C to 85°C (N version) |
| R5F6418MADFE (D) | | | | -40°C to 85°C (D version) |
| R5F6418MAPFE (D) | | | | -40°C to 85°C (P version) |
| R5F6418MANFD (P) | PLQP0144KA-A | 1 Mbyte + 8 Kbytes | 96 Kbytes | -20°C to 85°C (N version) |
| R5F6418MADFD (D) | | | | -40°C to 85°C (D version) |
| R5F6418MAPFD (D) | | | | -40°C to 85°C (P version) |

(D): Under development

(P): On planning phase

Notes:

1. The old package codes are as follows: PLQP0144KA-A: 144P6Q-A, PLQP0176KB-A: 176P6Q-A
2. Data flash memory provides an additional 8 Kbytes of ROM capacity.

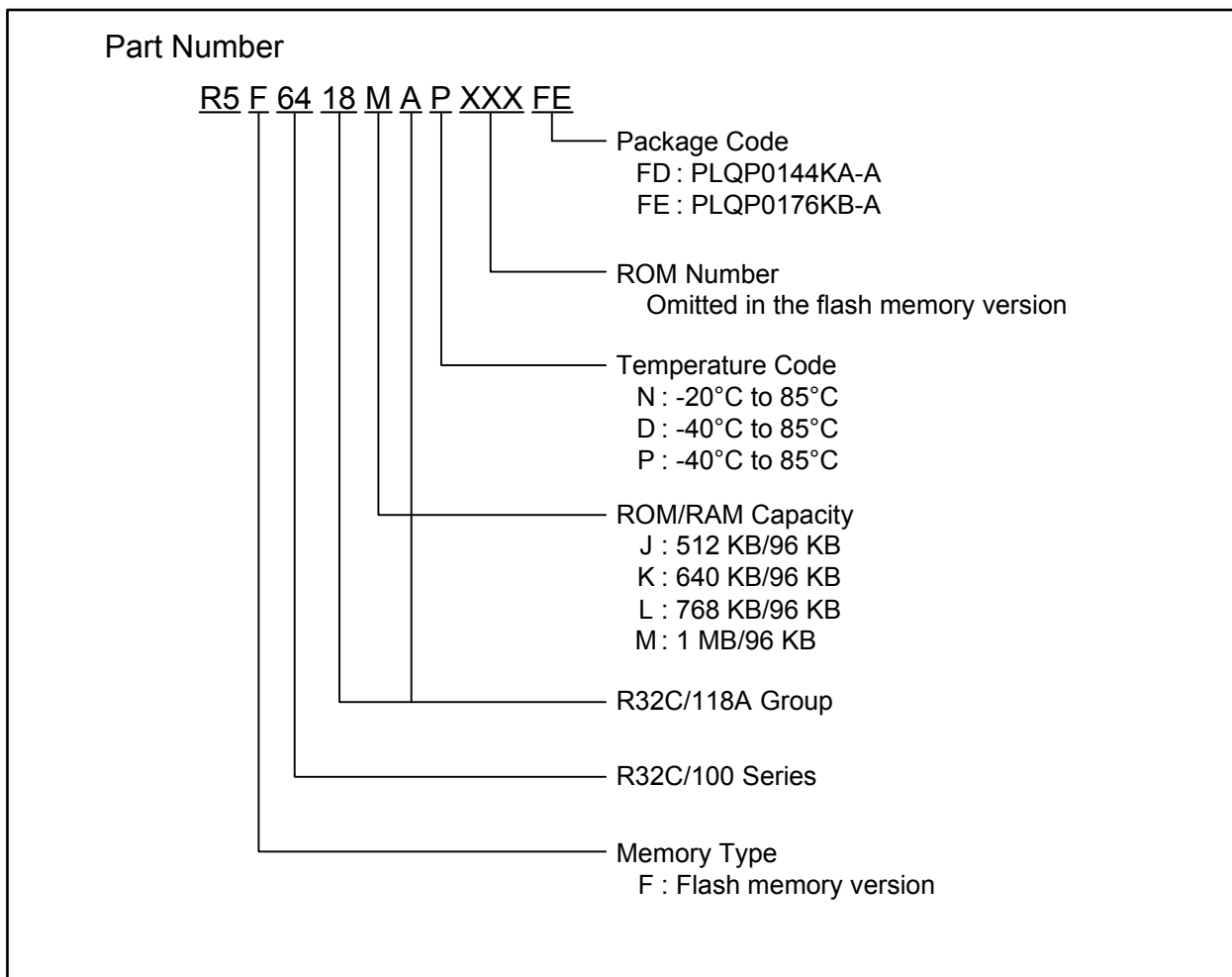


Figure 1.1 Part Numbering

1.3 Block Diagram

Figure 1.2 shows a block diagram of the R32C/118A Group.

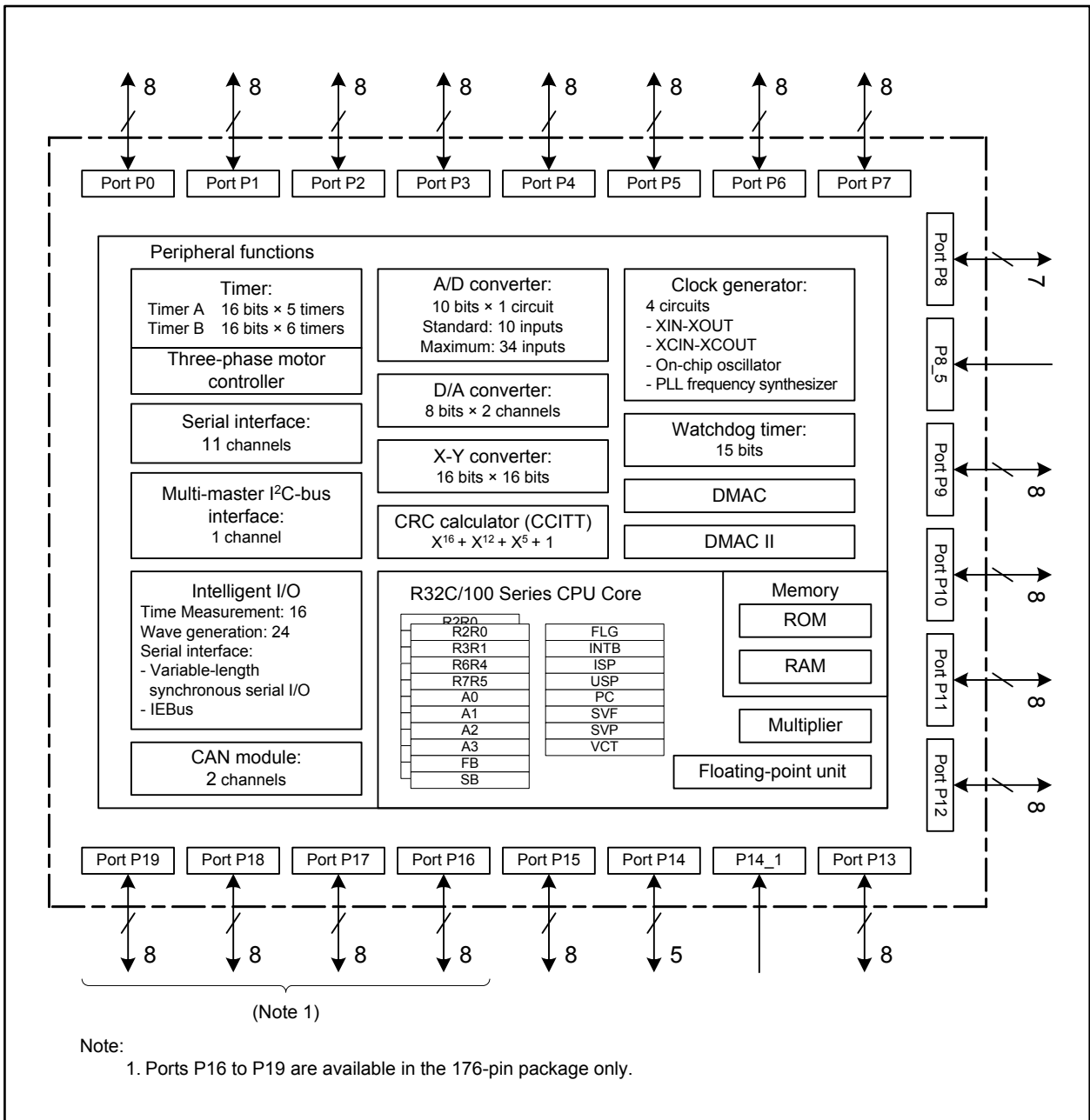


Figure 1.2 R32C/118A Group Block Diagram

Table 1.6 Pin Characteristics for the 176-pin Package (1/5)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|-------------|-------|---------------|-----------|---------------------------------------|--------------------------|------------|-----------------|
| 1 | | P9_6 | | | TXD4/SDA4/SRXD4/ CAN1OUT | | ANEX1 | |
| 2 | | P9_5 | | | CLK4/CAN1IN/ CAN1WU | | ANEX0 | |
| 3 | | P9_4 | | TB4IN | CTS4/RTS4/SS4 | | DA1 | |
| 4 | | P9_3 | | TB3IN | CTS3/RTS3/SS3 | | DA0 | |
| 5 | | P9_2 | | TB2IN | TXD3/SDA3/SRXD3 | OUTC2_0/ISTXD2/ IEOUT | | |
| 6 | | P9_1 | | TB1IN | RXD3/SCL3/STXD3 | ISRXD2/IEIN | | |
| 7 | | P9_0 | | TB0IN | CLK3 | | | |
| 8 | | P19_7 | | | | | | |
| 9 | | P14_6 | INT8 | | | | | |
| 10 | | P19_6 | | | | | | |
| 11 | | P14_5 | INT7 | | | | | |
| 12 | | P14_4 | INT6 | | | | | |
| 13 | | P14_3 | | | | | | |
| 14 | VDC0 | | | | | | | |
| 15 | | P14_1 | | | | | | |
| 16 | VDC1 | | | | | | | |
| 17 | NSD | | | | | | | |
| 18 | CNVSS | | | | | | | |
| 19 | XCIN | P8_7 | | | | | | |
| 20 | XCOU | P8_6 | | | | | | |
| 21 | RESET | | | | | | | |
| 22 | XOUT | | | | | | | |
| 23 | VSS | | | | | | | |
| 24 | XIN | | | | | | | |
| 25 | VCC | | | | | | | |
| 26 | | P8_5 | NMI | | | | | |
| 27 | | P8_4 | INT2 | | | | | |
| 28 | | P8_3 | INT1 | | CAN0IN/CAN0WU/ CAN1IN/CAN1WU | | | |
| 29 | | P8_2 | INT0 | | CAN0OUT/CAN1OUT | | | |
| 30 | | P8_1 | | TA4IN/U | CTS5/RTS5/SS5 | IIO1_5/UD0B/UD1B | | |
| 31 | | P8_0 | | TA4OUT/U | RXD5/SCL5/STXD5 | UD0A/UD1A | | |
| 32 | | P18_1 | | | | | | |
| 33 | | P18_0 | | | | | | |
| 34 | | P7_7 | | TA3IN | CLK5/CAN0IN/ CAN0WU | IIO1_4/UD0B/UD1B | | |
| 35 | | P7_6 | | TA3OUT | TXD5/SDA5/SRXD5/ CTS8/RTS8/CAN0OUT | IIO1_3/UD0A/UD1A | | |
| 36 | | P7_5 | | TA2IN/W | RXD8 | IIO1_2 | | |

Table 1.7 Pin Characteristics for the 176-pin Package (2/5)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|-------------|-------|---------------|------------------|--------------------------|---------------------------------|------------|--|
| 37 | | P7_4 | | TA2OUT/W | CLK8 | IIO1_1 | | |
| 38 | | P17_7 | | | | | | |
| 39 | | P17_6 | | | | | | |
| 40 | | P17_5 | | | | | | |
| 41 | | P17_4 | | | | | | |
| 42 | | P7_3 | | TA1IN/ \bar{V} | CTS2/RTS2/SS2/TXD8 | IIO1_0 | | |
| 43 | | P7_2 | | TA1OUT/V | CLK2 | | | |
| 44 | | P7_1 | | TB5IN/ TA0IN | RXD2/SCL2/STXD2/ MSCL | IIO1_7/OUTC2_2/ ISRXD2/IEIN | | |
| 45 | | P7_0 | | TA0OUT | TXD2/SDA2/SRXD2/ MSDA | IIO1_6/OUTC2_0/ ISTXD2/IEOUT | | |
| 46 | | P6_7 | | | TXD1/SDA1/SRXD1 | | | |
| 47 | | P14_7 | | | | | | |
| 48 | | P6_6 | | | RXD1/SCL1/STXD1 | | | |
| 49 | | P11_7 | | | | | | |
| 50 | | P6_5 | | | CLK1 | | | |
| 51 | | P6_4 | | | CTS1/RTS1/SS1 | OUTC2_1/ISCLK2 | | |
| 52 | | P6_3 | | | TXD0/SDA0/SRXD0 | | | |
| 53 | | P6_2 | | TB2IN | RXD0/SCL0/STXD0 | | | |
| 54 | | P6_1 | | TB1IN | CLK0 | | | |
| 55 | | P6_0 | | TB0IN | CTS0/RTS0/SS0 | | | |
| 56 | | P19_5 | | | | | | |
| 57 | | P13_7 | | | | OUTC2_7 | | D31 |
| 58 | | P13_6 | | | | OUTC2_1/ISCLK2 | | D30 |
| 59 | | P13_5 | | | | OUTC2_2/ISRXD2/ IEIN | | D29 |
| 60 | | P13_4 | | | | OUTC2_0/ISTXD2/ IEOUT | | D28 |
| 61 | | P19_4 | | | | | | |
| 62 | | P5_7 | | | CTS7/RTS7 | | | $\overline{\text{RDY}}/\overline{\text{CS3}}$ |
| 63 | | P5_6 | | | RXD7 | | | $\overline{\text{ALE}}/\overline{\text{CS2}}$ |
| 64 | | P5_5 | | | CLK7 | | | $\overline{\text{HOLD}}$ |
| 65 | | P5_4 | | | TXD7 | | | $\overline{\text{HLDA}}/\overline{\text{CS1}}$ |
| 66 | | P13_3 | | | | OUTC2_3 | | D27 |
| 67 | VSS | | | | | | | |
| 68 | | P13_2 | | | | OUTC2_6 | | D26 |
| 69 | VCC | | | | | | | |
| 70 | | P13_1 | | | | OUTC2_5 | | D25 |
| 71 | | P13_0 | | | | OUTC2_4 | | D24 |
| 72 | | P5_3 | | | | | | CLKOUT/ BCLK |
| 73 | | P5_2 | | | | | | $\overline{\text{RD}}$ |
| 74 | | P5_1 | | | | | | $\overline{\text{WR1}}/\overline{\text{BC1}}$ |

Table 1.8 Pin Characteristics for the 176-pin Package (3/5)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|-------------|-------|---------------|------------------|---------------------|--------------------------|------------|-----------------|
| 75 | | P5_0 | | | | | | WR0/WR |
| 76 | | P12_7 | | | | | | D23 |
| 77 | | P12_6 | | | | | | D22 |
| 78 | | P12_5 | | | | | | D21 |
| 79 | | P19_3 | | | | | | |
| 80 | | P17_3 | | | | | | |
| 81 | | P17_2 | | | | | | |
| 82 | | P17_1 | | | | | | |
| 83 | | P17_0 | | | | | | |
| 84 | | P19_2 | | | | | | |
| 85 | | P4_7 | | | TXD6/SDA6/SRXD6 | | | CS0/A23 |
| 86 | | P4_6 | | | RXD6/SCL6/STXD6 | | | CS1/A22 |
| 87 | | P4_5 | | | CLK6 | | | CS2/A21 |
| 88 | | P4_4 | | | CTS6/RTS6/SS6 | | | CS3/A20 |
| 89 | | P4_3 | | | TXD3/SDA3/SRXD3 | OUTC2_0/ISTXD2/ IEOUT | | A19 |
| 90 | | P11_6 | | | | | | |
| 91 | | P4_2 | | | RXD3/SCL3/STXD3 | ISRXD2/IEIN | | A18 |
| 92 | | P11_5 | | | | | | |
| 93 | | P4_1 | | | CLK3 | | | A17 |
| 94 | | P4_0 | | | CTS3/RTS3/SS3 | | | A16 |
| 95 | | P16_7 | | | TXD10 | | | |
| 96 | | P16_6 | | | RXD10 | | | |
| 97 | | P16_5 | | | CLK10 | | | |
| 98 | | P16_4 | | | CTS10/RTS10 | | | |
| 99 | | P3_7 | | TA4IN/ \bar{U} | | | | A15/(D15) |
| 100 | | P3_6 | | TA4OUT/U | | | | A14/(D14) |
| 101 | | P3_5 | | TA2IN/ \bar{W} | | | | A13/(D13) |
| 102 | | P3_4 | | TA2OUT/W | | | | A12/(D12) |
| 103 | | P16_3 | | | TXD9 | | | |
| 104 | | P16_2 | | | RXD9 | | | |
| 105 | | P16_1 | | | CLK9 | | | |
| 106 | | P16_0 | | | CTS9/RTS9 | | | |
| 107 | | P3_3 | | TA1IN/ \bar{V} | | | | A11/(D11) |
| 108 | | P3_2 | | TA1OUT/V | | | | A10/(D10) |
| 109 | | P3_1 | | TA3OUT | | UD0B/UD1B | | A9/(D9) |
| 110 | | P12_4 | | | | | | D20 |
| 111 | | P12_3 | | | CTS6/RTS6/SS6 | | | D19 |
| 112 | | P12_2 | | | RXD6/SCL6/STXD6 | | | D18 |
| 113 | | P12_1 | | | CLK6 | | | D17 |
| 114 | | P12_0 | | | TXD6/SDA6/SRXD6 | | | D16 |

Table 1.9 Pin Characteristics for the 176-pin Package (4/5)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|-------------|-------|---------------|-----------|---------------------|---------------------|------------|----------------------|
| 115 | VCC | | | | | | | |
| 116 | | P3_0 | | TA0OUT | | UD0A/UD1A | | A8(/D8) |
| 117 | VSS | | | | | | | |
| 118 | | P2_7 | | | TXD10 | | AN2_7 | A7(/D7) |
| 119 | | P2_6 | | | RXD10 | | AN2_6 | A6(/D6) |
| 120 | | P2_5 | | | CLK10 | | AN2_5 | A5(/D5) |
| 121 | | P2_4 | | | CTS10/RTS10 | | AN2_4 | A4(/D4) |
| 122 | | P2_3 | | | TXD9 | | AN2_3 | A3(/D3) |
| 123 | | P2_2 | | | RXD9 | | AN2_2 | A2(/D2) |
| 124 | | P2_1 | | | CLK9 | | AN2_1 | A1(/D1)/ BC2(/D1) |
| 125 | | P2_0 | | | CTS9/RTS9 | | AN2_0 | A0(/D0)/ BC0(/D0) |
| 126 | | P1_7 | INT5 | | | IIO0_7/IIO1_7 | | D15 |
| 127 | | P1_6 | INT4 | | | IIO0_6/IIO1_6 | | D14 |
| 128 | | P1_5 | INT3 | | | IIO0_5/IIO1_5 | | D13 |
| 129 | | P1_4 | | | | IIO0_4/IIO1_4 | | D12 |
| 130 | | P1_3 | | | | IIO0_3/IIO1_3 | | D11 |
| 131 | | P1_2 | | | | IIO0_2/IIO1_2 | | D10 |
| 132 | | P1_1 | | | | IIO0_1/IIO1_1 | | D9 |
| 133 | | P1_0 | | | | IIO0_0/IIO1_0 | | D8 |
| 134 | | P0_7 | | | | | AN0_7 | D7 |
| 135 | | P0_6 | | | | | AN0_6 | D6 |
| 136 | | P0_5 | | | | | AN0_5 | D5 |
| 137 | | P0_4 | | | | | AN0_4 | D4 |
| 138 | | P19_1 | | | | | | |
| 139 | | P11_4 | | | | | | BC3/WR3 |
| 140 | | P19_0 | | | | | | |
| 141 | | P11_3 | | | CTS8/RTS8 | IIO1_3 | | CS3/WR2 |
| 142 | | P11_2 | | | RXD8 | IIO1_2 | | CS2 |
| 143 | | P11_1 | | | CLK8 | IIO1_1 | | CS1 |
| 144 | | P11_0 | | | TXD8 | IIO1_0 | | CS0 |
| 145 | | P18_7 | | | | | | |
| 146 | | P18_6 | | | | | | |
| 147 | | P18_5 | | | | | | |
| 148 | | P18_4 | | | | | | |
| 149 | | P18_3 | | | | | | |
| 150 | | P18_2 | | | | | | |
| 151 | | P0_3 | | | | | AN0_3 | D3 |
| 152 | | P0_2 | | | | | AN0_2 | D2 |
| 153 | | P0_1 | | | | | AN0_1 | D1 |
| 154 | | P0_0 | | | | | AN0_0 | D0 |
| 155 | | P15_7 | | | CTS6/RTS6/SS6 | IIO0_7 | AN15_7 | |

Table 1.10 Pin Characteristics for the 176-pin Package (5/5)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|-------------|-------|-------------------------|-----------|---------------------|---------------------|---------------------------|-----------------|
| 156 | | P15_6 | | | CLK6 | IIO0_6 | AN15_6 | |
| 157 | | P15_5 | | | RXD6/SCL6/STXD6 | IIO0_5 | AN15_5 | |
| 158 | | P15_4 | | | TXD6/SDA6/SRXD6 | IIO0_4 | AN15_4 | |
| 159 | | P15_3 | | | CTS7/RTS7 | IIO0_3 | AN15_3 | |
| 160 | | P15_2 | | | RXD7 | IIO0_2 | AN15_2 | |
| 161 | | P15_1 | | | CLK7 | IIO0_1 | AN15_1 | |
| 162 | VSS | | | | | | | |
| 163 | | P15_0 | | | TXD7 | IIO0_0 | AN15_0 | |
| 164 | VCC | | | | | | | |
| 165 | | P10_7 | $\overline{\text{KI3}}$ | | | | AN_7 | |
| 166 | | P10_6 | $\overline{\text{KI2}}$ | | | | AN_6 | |
| 167 | | P10_5 | $\overline{\text{KI1}}$ | | | | AN_5 | |
| 168 | | P10_4 | $\overline{\text{KI0}}$ | | | | AN_4 | |
| 169 | | P10_3 | | | | | AN_3 | |
| 170 | | P10_2 | | | | | AN_2 | |
| 171 | | P10_1 | | | | | AN_1 | |
| 172 | AVSS | | | | | | | |
| 173 | | P10_0 | | | | | AN_0 | |
| 174 | VREF | | | | | | | |
| 175 | AVCC | | | | | | | |
| 176 | | P9_7 | | | RXD4/SCL4/STXD4 | | $\overline{\text{ADTRG}}$ | |

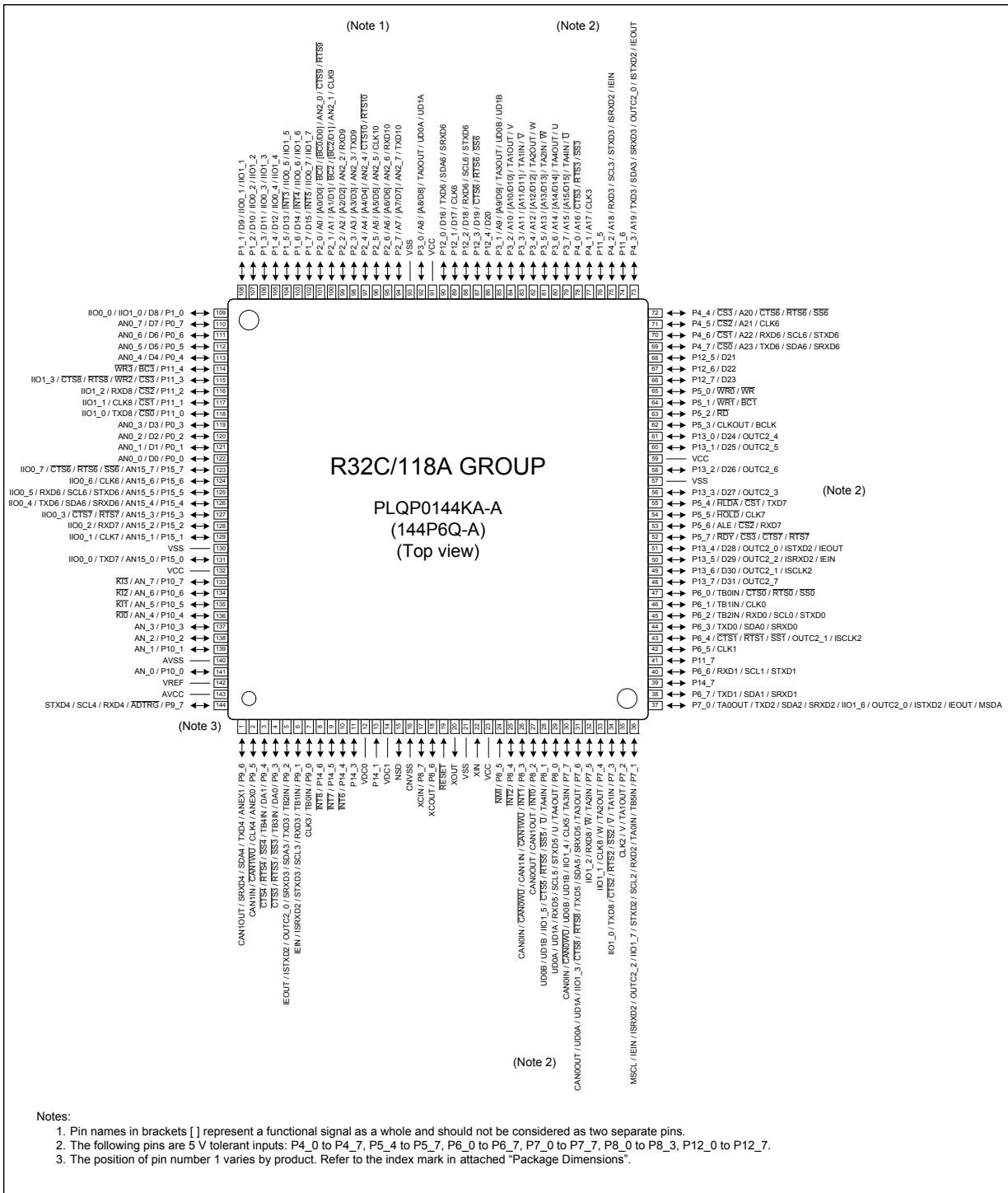


Figure 1.4 Pin Assignment for the 144-pin Package (top view)

Table 1.11 Pin Characteristics for the 144-pin Package (1/4)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|---------------------------|-------|--------------------------|------------------------------|---|--------------------------------|------------|-----------------|
| 1 | | P9_6 | | | TXD4/SDA4/SRXD4/ CAN1OUT | | ANEX1 | |
| 2 | | P9_5 | | | CLK4/CAN1IN/ CAN1WU | | ANEX0 | |
| 3 | | P9_4 | | TB4IN | $\overline{\text{CTS4}}/\text{RTS4}/\overline{\text{SS4}}$ | | DA1 | |
| 4 | | P9_3 | | TB3IN | $\overline{\text{CTS3}}/\text{RTS3}/\overline{\text{SS3}}$ | | DA0 | |
| 5 | | P9_2 | | TB2IN | TXD3/SDA3/SRXD3 | OUTC2_0/ISTXD2/ IEOUT | | |
| 6 | | P9_1 | | TB1IN | RXD3/SCL3/STXD3 | ISRXD2/IEIN | | |
| 7 | | P9_0 | | TB0IN | CLK3 | | | |
| 8 | | P14_6 | INT8 | | | | | |
| 9 | | P14_5 | $\overline{\text{INT7}}$ | | | | | |
| 10 | | P14_4 | INT6 | | | | | |
| 11 | | P14_3 | | | | | | |
| 12 | VDC0 | | | | | | | |
| 13 | | P14_1 | | | | | | |
| 14 | VDC1 | | | | | | | |
| 15 | NSD | | | | | | | |
| 16 | CNVSS | | | | | | | |
| 17 | XCIN | P8_7 | | | | | | |
| 18 | XCOU | P8_6 | | | | | | |
| 19 | $\overline{\text{RESET}}$ | | | | | | | |
| 20 | XOUT | | | | | | | |
| 21 | VSS | | | | | | | |
| 22 | XIN | | | | | | | |
| 23 | VCC | | | | | | | |
| 24 | | P8_5 | NMI | | | | | |
| 25 | | P8_4 | $\overline{\text{INT2}}$ | | | | | |
| 26 | | P8_3 | INT1 | | CAN0IN/CAN0WU/ CAN1IN/CAN1WU | | | |
| 27 | | P8_2 | $\overline{\text{INT0}}$ | | CAN0OUT/CAN1OUT | | | |
| 28 | | P8_1 | | TA4IN/ $\overline{\text{U}}$ | $\overline{\text{CTS5}}/\text{RTS5}/\overline{\text{SS5}}$ | IIO1_5/UD0B/UD1B | | |
| 29 | | P8_0 | | TA4OUT/U | RXD5/SCL5/STXD5 | UD0A/UD1A | | |
| 30 | | P7_7 | | TA3IN | CLK5/CAN0IN/ CAN0WU | IIO1_4/UD0B/UD1B | | |
| 31 | | P7_6 | | TA3OUT | TXD5/SDA5/SRXD5/ $\overline{\text{CTS8}}/\text{RTS8}/\text{CAN0OUT}$ | IIO1_3/UD0A/UD1A | | |
| 32 | | P7_5 | | TA2IN/ $\overline{\text{W}}$ | RXD8 | IIO1_2 | | |
| 33 | | P7_4 | | TA2OUT/W | CLK8 | IIO1_1 | | |
| 34 | | P7_3 | | TA1IN/ $\overline{\text{V}}$ | $\overline{\text{CTS2}}/\text{RTS2}/\overline{\text{SS2}}/\text{TXD8}$ | IIO1_0 | | |
| 35 | | P7_2 | | TA1OUT/V | CLK2 | | | |
| 36 | | P7_1 | | TB5IN/ TA0IN | RXD2/SCL2/STXD2/ MSCL | IIO1_7/OUTC2_2/ ISRXD2/IEIN | | |

Table 1.12 Pin Characteristics for the 144-pin Package (2/4)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|-------------|-------|---------------|-----------|--------------------------|---------------------------------|------------|-----------------|
| 37 | | P7_0 | | TA0OUT | TXD2/SDA2/SRXD2/ MSDA | IIO1_6/OUTC2_0/ ISTXD2/IEOUT | | |
| 38 | | P6_7 | | | TXD1/SDA1/SRXD1 | | | |
| 39 | | P14_7 | | | | | | |
| 40 | | P6_6 | | | RXD1/SCL1/STXD1 | | | |
| 41 | | P11_7 | | | | | | |
| 42 | | P6_5 | | | CLK1 | | | |
| 43 | | P6_4 | | | CTS1/RTS1/SS1 | OUTC2_1/ISCLK2 | | |
| 44 | | P6_3 | | | TXD0/SDA0/SRXD0 | | | |
| 45 | | P6_2 | | TB2IN | RXD0/SCL0/STXD0 | | | |
| 46 | | P6_1 | | TB1IN | CLK0 | | | |
| 47 | | P6_0 | | TB0IN | CTS0/RTS0/SS0 | | | |
| 48 | | P13_7 | | | | OUTC2_7 | | D31 |
| 49 | | P13_6 | | | | OUTC2_1/ISCLK2 | | D30 |
| 50 | | P13_5 | | | | OUTC2_2/ISRXD2/ IEIN | | D29 |
| 51 | | P13_4 | | | | OUTC2_0/ISTXD2/ IEOUT | | D28 |
| 52 | | P5_7 | | | CTS7/RTS7 | | | RDY/CS3 |
| 53 | | P5_6 | | | RXD7 | | | ALE/CS2 |
| 54 | | P5_5 | | | CLK7 | | | HOLD |
| 55 | | P5_4 | | | TXD7 | | | HLDA/CS1 |
| 56 | | P13_3 | | | | OUTC2_3 | | D27 |
| 57 | VSS | | | | | | | |
| 58 | | P13_2 | | | | OUTC2_6 | | D26 |
| 59 | VCC | | | | | | | |
| 60 | | P13_1 | | | | OUTC2_5 | | D25 |
| 61 | | P13_0 | | | | OUTC2_4 | | D24 |
| 62 | | P5_3 | | | | | | CLKOUT/ BCLK |
| 63 | | P5_2 | | | | | | RD |
| 64 | | P5_1 | | | | | | WR1/BC1 |
| 65 | | P5_0 | | | | | | WR0/WR |
| 66 | | P12_7 | | | | | | D23 |
| 67 | | P12_6 | | | | | | D22 |
| 68 | | P12_5 | | | | | | D21 |
| 69 | | P4_7 | | | TXD6/SDA6/SRXD6 | | | CS0/A23 |
| 70 | | P4_6 | | | RXD6/SCL6/STXD6 | | | CS1/A22 |
| 71 | | P4_5 | | | CLK6 | | | CS2/A21 |
| 72 | | P4_4 | | | CTS6/RTS6/SS6 | | | CS3/A20 |
| 73 | | P4_3 | | | TXD3/SDA3/SRXD3 | OUTC2_0/ISTXD2/ IEOUT | | A19 |
| 74 | | P11_6 | | | | | | |

Table 1.13 Pin Characteristics for the 144-pin Package (3/4)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|-------------|-------|---------------|-----------|---------------------|---------------------|------------|----------------------|
| 75 | | P4_2 | | | RXD3/SCL3/STXD3 | ISRXD2/IEIN | | A18 |
| 76 | | P11_5 | | | | | | |
| 77 | | P4_1 | | | CLK3 | | | A17 |
| 78 | | P4_0 | | | CTS3/RTS3/SS3 | | | A16 |
| 79 | | P3_7 | | TA4IN/U | | | | A15/(D15) |
| 80 | | P3_6 | | TA4OUT/U | | | | A14/(D14) |
| 81 | | P3_5 | | TA2IN/W | | | | A13/(D13) |
| 82 | | P3_4 | | TA2OUT/W | | | | A12/(D12) |
| 83 | | P3_3 | | TA1IN/V | | | | A11/(D11) |
| 84 | | P3_2 | | TA1OUT/V | | | | A10/(D10) |
| 85 | | P3_1 | | TA3OUT | | UD0B/UD1B | | A9/(D9) |
| 86 | | P12_4 | | | | | | D20 |
| 87 | | P12_3 | | | CTS6/RTS6/SS6 | | | D19 |
| 88 | | P12_2 | | | RXD6/SCL6/STXD6 | | | D18 |
| 89 | | P12_1 | | | CLK6 | | | D17 |
| 90 | | P12_0 | | | TXD6/SDA6/SRXD6 | | | D16 |
| 91 | VCC | | | | | | | |
| 92 | | P3_0 | | TA0OUT | | UD0A/UD1A | | A8/(D8) |
| 93 | VSS | | | | | | | |
| 94 | | P2_7 | | | TXD10 | | AN2_7 | A7/(D7) |
| 95 | | P2_6 | | | RXD10 | | AN2_6 | A6/(D6) |
| 96 | | P2_5 | | | CLK10 | | AN2_5 | A5/(D5) |
| 97 | | P2_4 | | | CTS10/RTS10 | | AN2_4 | A4/(D4) |
| 98 | | P2_3 | | | TXD9 | | AN2_3 | A3/(D3) |
| 99 | | P2_2 | | | RXD9 | | AN2_2 | A2/(D2) |
| 100 | | P2_1 | | | CLK9 | | AN2_1 | A1/(D1)/ BC2/(D1) |
| 101 | | P2_0 | | | CTS9/RTS9 | | AN2_0 | A0/(D0)/ BC0/(D0) |
| 102 | | P1_7 | INT5 | | | IIO0_7/IIO1_7 | | D15 |
| 103 | | P1_6 | INT4 | | | IIO0_6/IIO1_6 | | D14 |
| 104 | | P1_5 | INT3 | | | IIO0_5/IIO1_5 | | D13 |
| 105 | | P1_4 | | | | IIO0_4/IIO1_4 | | D12 |
| 106 | | P1_3 | | | | IIO0_3/IIO1_3 | | D11 |
| 107 | | P1_2 | | | | IIO0_2/IIO1_2 | | D10 |
| 108 | | P1_1 | | | | IIO0_1/IIO1_1 | | D9 |
| 109 | | P1_0 | | | | IIO0_0/IIO1_0 | | D8 |
| 110 | | P0_7 | | | | | AN0_7 | D7 |
| 111 | | P0_6 | | | | | AN0_6 | D6 |

Table 1.14 Pin Characteristics for the 144-pin Package (4/4)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Module Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin |
|---------|-------------|-------|---------------|-----------|---------------------|---------------------|------------|-----------------|
| 112 | | P0_5 | | | | | AN0_5 | D5 |
| 113 | | P0_4 | | | | | AN0_4 | D4 |
| 114 | | P11_4 | | | | | | BC3/WR3 |
| 115 | | P11_3 | | | CTS8/RTS8 | IIO1_3 | | CS3/WR2 |
| 116 | | P11_2 | | | RXD8 | IIO1_2 | | CS2 |
| 117 | | P11_1 | | | CLK8 | IIO1_1 | | CS1 |
| 118 | | P11_0 | | | TXD8 | IIO1_0 | | CS0 |
| 119 | | P0_3 | | | | | AN0_3 | D3 |
| 120 | | P0_2 | | | | | AN0_2 | D2 |
| 121 | | P0_1 | | | | | AN0_1 | D1 |
| 122 | | P0_0 | | | | | AN0_0 | D0 |
| 123 | | P15_7 | | | CTS6/RTS6/SS6 | IIO0_7 | AN15_7 | |
| 124 | | P15_6 | | | CLK6 | IIO0_6 | AN15_6 | |
| 125 | | P15_5 | | | RXD6/SCL6/STXD6 | IIO0_5 | AN15_5 | |
| 126 | | P15_4 | | | TXD6/SDA6/SRXD6 | IIO0_4 | AN15_4 | |
| 127 | | P15_3 | | | CTS7/RTS7 | IIO0_3 | AN15_3 | |
| 128 | | P15_2 | | | RXD7 | IIO0_2 | AN15_2 | |
| 129 | | P15_1 | | | CLK7 | IIO0_1 | AN15_1 | |
| 130 | VSS | | | | | | | |
| 131 | | P15_0 | | | TXD7 | IIO0_0 | AN15_0 | |
| 132 | VCC | | | | | | | |
| 133 | | P10_7 | KI3 | | | | AN_7 | |
| 134 | | P10_6 | KI2 | | | | AN_6 | |
| 135 | | P10_5 | KI1 | | | | AN_5 | |
| 136 | | P10_4 | KI0 | | | | AN_4 | |
| 137 | | P10_3 | | | | | AN_3 | |
| 138 | | P10_2 | | | | | AN_2 | |
| 139 | | P10_1 | | | | | AN_1 | |
| 140 | AVSS | | | | | | | |
| 141 | | P10_0 | | | | | AN_0 | |
| 142 | VREF | | | | | | | |
| 143 | AVCC | | | | | | | |
| 144 | | P9_7 | | | RXD4/SCL4/STXD4 | | ADTRG | |

1.5 Pin Definitions and Functions

Table 1.15 to Table 1.19 show the pin definitions and functions.

Table 1.15 Pin Definitions and Functions (1/4)

| Function | Symbol | I/O | Description |
|--|--|-----|---|
| Power supply | VCC, VSS | I | Applicable as follows: VCC = 3.0 to 5.5 V, VSS = 0 V |
| Connecting pins for decoupling capacitor | VDC0, VDC1 | — | A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1 |
| Analog power supply | AVCC, AVSS | I | Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively |
| Reset input | $\overline{\text{RESET}}$ | I | The MCU is reset when this pin is driven low |
| CNVSS | CNVSS | I | This pin should be connected to VSS via a resistor |
| Debug port | NSD | I/O | This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 k Ω |
| Main clock input | XIN | I | Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open |
| Main clock output | XOUT | O | |
| Sub clock input | XCIN | I | Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOU. An external clock should be input at the XCIN while leaving the XCOU open |
| Sub clock output | XCOU | O | |
| BCLK output | BCLK | O | BCLK output |
| Clock output | CLKOUT | O | Output of the clock with the same frequency as low speed clocks, f8, or f32 |
| External interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT8}}$ | I | Input for external interrupts |
| NMI input | P8_5/ $\overline{\text{NMI}}$ | I | Input for NMI |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Input for the key input interrupt |
| Bus control pins | D0 to D7 | I/O | Input/output of data (D0 to D7) while accessing an external memory space with a separate bus |
| | D8 to D15 | I/O | Input/output of data (D8 to D15) while accessing an external memory space with 16-bit or 32-bit separate bus |
| | D16 to D31 | I/O | Input/output of data (D16 to D31) while accessing an external memory space with 32-bit separate bus |
| | A0 to A23 | O | Output of address bits A0 to A23 |
| | A0/D0 to A7/D7 | I/O | Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus |
| | A8/D8 to A15/D15 | I/O | Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit or 32-bit multiplexed bus |

Table 1.16 Pin Definitions and Functions (2/4)

| Function | Symbol | I/O | Description |
|------------------|---|---|--|
| Bus control pins | $\overline{BC0}/D0, \overline{BC2}/D1$ | I/O | Output of byte control ($\overline{BC0}$ and $\overline{BC2}$) and input/output of data (D0 and D1) by time-division while accessing an external memory space with multiplexed bus |
| | $\overline{CS0}$ to $\overline{CS3}$ | O | Chip select output |
| | $\overline{WR0}/\overline{WR1}/\overline{WR2}/\overline{WR3},$ $\overline{WR}/\overline{BC0}/\overline{BC1}/\overline{BC2}/\overline{BC3},$ \overline{RD} | O | Output of write, byte control, and read signals. Either \overline{WRx} or \overline{WR} and \overline{BCx} can be selected by a program. Data is read when \overline{RD} is low. <ul style="list-style-type: none"> • When $\overline{WR0}, \overline{WR1}, \overline{WR2}, \overline{WR3},$ and \overline{RD} are selected, data is written to the following address: 4n+0, when $\overline{WR0}$ is low 4n+1, when $\overline{WR1}$ is low 4n+2, when $\overline{WR2}$ is low 4n+3, when $\overline{WR3}$ is low on 32-bit external data bus or an even address, when $\overline{WR0}$ is low an odd address, when $\overline{WR1}$ is low on 16-bit external data bus • When $\overline{WR}, \overline{BC0}, \overline{BC1}, \overline{BC2}, \overline{BC3},$ and \overline{RD} are selected, data is written, when \overline{WR} is low and the following address is accessed: 4n+0, when $\overline{BC0}$ is low 4n+1, when $\overline{BC1}$ is low 4n+2, when $\overline{BC2}$ is low 4n+3, when $\overline{BC3}$ is low on 32-bit external data bus or an even address, when $\overline{BC0}$ is low an odd address, when $\overline{BC1}$ is low on 16-bit external data bus |
| | ALE | O | Latch enable signal in multiplexed bus format |
| | \overline{HOLD} | I | The MCU is in a hold state while this pin is held low |
| | \overline{HLDA} | O | This pin is driven low while the MCU is held in a hold state |
| \overline{RDY} | I | Bus cycle is extended by the CPU if this pin is low on the falling edge of the BCLK | |

Table 1.17 Pin Definitions and Functions (3/4)

| Function | Symbol | I/O | Description |
|--|--|-----|--|
| I/O port (1) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 | I/O | I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Some ports are 5 V tolerant inputs. Pull-up resistors and N-channel open drain setting can be enabled on some ports. Refer to Table 1.19 "Pin Specifications" for details |
| Input port | P14_1 | I | Input port in CMOS Pull-up resistor is selectable. Refer to Table 1.19 "Pin Specifications" for details |
| Timer A | TA0OUT to TA4OUT | I/O | Timers A0 to A4 input/output |
| | TA0IN to TA4IN | I | Timers A0 to A4 input |
| Timer B | TB0IN to TB5IN | I | Timers B0 to B5 input |
| Three-phase motor control timer output | U, \bar{U} , V, \bar{V} , W, \bar{W} | O | Three-phase motor control timer output |
| Serial interface | $\overline{\text{CTS0}}$ to $\overline{\text{CTS10}}$ | I | Handshake input |
| | $\overline{\text{RTS0}}$ to $\overline{\text{RTS10}}$ | O | Handshake output |
| | CLK0 to CLK10 | I/O | Transmit/receive clock input/output |
| | RXD0 to RXD10 | I | Serial data input |
| | TXD0 to TXD10 | O | Serial data output |
| I ² C bus (simplified) | SDA0 to SDA6 | I/O | Serial data input/output |
| | SCL0 to SCL6 | I/O | Transmit/receive clock input/output |
| Serial interface special functions | STXD0 to STXD6 | O | Serial data output in slave mode |
| | SRXD0 to SRXD6 | I | Serial data input in slave mode |
| | $\overline{\text{SS0}}$ to $\overline{\text{SS6}}$ | I | Input to control serial interface special functions |

Note:

- Ports P16 to P19 are available in the 176-pin package only.

Table 1.18 Pin Definitions and Functions (4/4)

| Function | Symbol | I/O | Description |
|-----------------------------------|--|-----|--|
| A/D converter | AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7 | I | Analog input for the A/D converter |
| | ADTRG | I | External trigger input for the A/D converter |
| | ANEX0 | I/O | Expanded analog input for the A/D converter and output in external op-amp connection mode |
| | ANEX1 | I | Expanded analog input for the A/D converter |
| D/A converter | DA0, DA1 | O | Output for the D/A converter |
| Reference voltage input | VREF | I | Reference voltage input for the A/D converter and D/A converter |
| Intelligent I/O | IIO0_0 to IIO0_7 | I/O | Input/output for the Intelligent I/O group 0. Either input capture or output compare is selectable |
| | IIO1_0 to IIO1_7 | I/O | Input/output for the Intelligent I/O group 1. Either input capture or output compare is selectable |
| | UD0A, UD0B, UD1A, UD1B | I | Input for the two-phase encoder |
| | OUTC2_0 to OUTC2_7 | O | Output for OC (output compare) of the Intelligent I/O group 2 |
| | ISCLK2 | I/O | Clock input/output for the serial interface |
| | ISRXD2 | I | Receive data input for the serial interface |
| | ISTXD2 | O | Transmit data output for the serial interface |
| | IEIN | I | Receive data input for the serial interface |
| | IEOUT | O | Transmit data output for the serial interface |
| Multi-master I ² C-bus | MSDA | I/O | Serial data input/output |
| | MSCL | I/O | Transmit/receive clock input/output |
| CAN Module | CAN0IN, CAN1IN | I | Receive data input for the CAN communications |
| | CAN0OUT, CAN1OUT | O | Transmit data output for the CAN communications |
| | CAN0WU, CAN1WU | I | Input for the CAN wake-up interrupt |

Table 1.19 Pin Specifications

| Pin names | Package | | Selectable Functions | | 5 V tolerant input ⁽³⁾ |
|------------------|---------|---------|---------------------------------|-------------------------------------|-----------------------------------|
| | 176-pin | 144-pin | Pull-up resistor ⁽¹⁾ | N-channel open drain ⁽²⁾ | |
| P0_0 to P0_7 | ✓ | ✓ | ✓ | | |
| P1_0 to P1_7 | ✓ | ✓ | ✓ | | |
| P2_0 to P2_7 | ✓ | ✓ | ✓ | | |
| P3_0 to P3_7 | ✓ | ✓ | ✓ | | |
| P4_0 to P4_7 | ✓ | ✓ | | ✓ | ✓ |
| P5_0 to P5_3 | ✓ | ✓ | ✓ | | |
| P5_4 to P5_7 | ✓ | ✓ | | ✓ | ✓ |
| P6_0 to P6_7 | ✓ | ✓ | | ✓ | ✓ |
| P7_0 to P7_7 | ✓ | ✓ | | ✓ | ✓ |
| P8_0 to P8_3 | ✓ | ✓ | | ✓ | ✓ |
| P8_4, P8_6, P8_7 | ✓ | ✓ | ✓ | | |
| P9_0 to P9_7 | ✓ | ✓ | ✓ | ✓ | |
| P10_0 to P10_7 | ✓ | ✓ | ✓ | | |
| P11_0 to P11_3 | ✓ | ✓ | ✓ | ✓ | |
| P11_4 to P11_7 | ✓ | ✓ | ✓ | | |
| P12_0 to P12_7 | ✓ | ✓ | | ✓ | ✓ |
| P13_0 to P13_7 | ✓ | ✓ | ✓ | | |
| P14_1, P14_3 | ✓ | ✓ | ✓ | | |
| P14_4 to P14_7 | ✓ | ✓ | ✓ | | |
| P15_0 to P15_7 | ✓ | ✓ | ✓ | ✓ | |
| P16_0 to P16_7 | ✓ | | | ✓ | ✓ |
| P17_0 to P17_3 | ✓ | | | ✓ | ✓ |
| P17_4 to P17_7 | ✓ | | ✓ | | |
| P18_0 to P18_7 | ✓ | | ✓ | | |
| P19_0 to P19_7 | ✓ | | ✓ | | |

Notes:

1. Pull-up resistors are selected in 4-pin units, but are only enabled for those pins set as input ports.
2. N-channel open drain output can be enabled on the applicable pins on a discrete pin basis.
3. 5 V tolerant input is enabled when an applicable pin is set as an input port. When it is set as an I/O port, to enable 5 V tolerant input, this pin should be set as N-channel open drain output.

2. Central Processing Unit (CPU)

The CPU contains registers as shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.

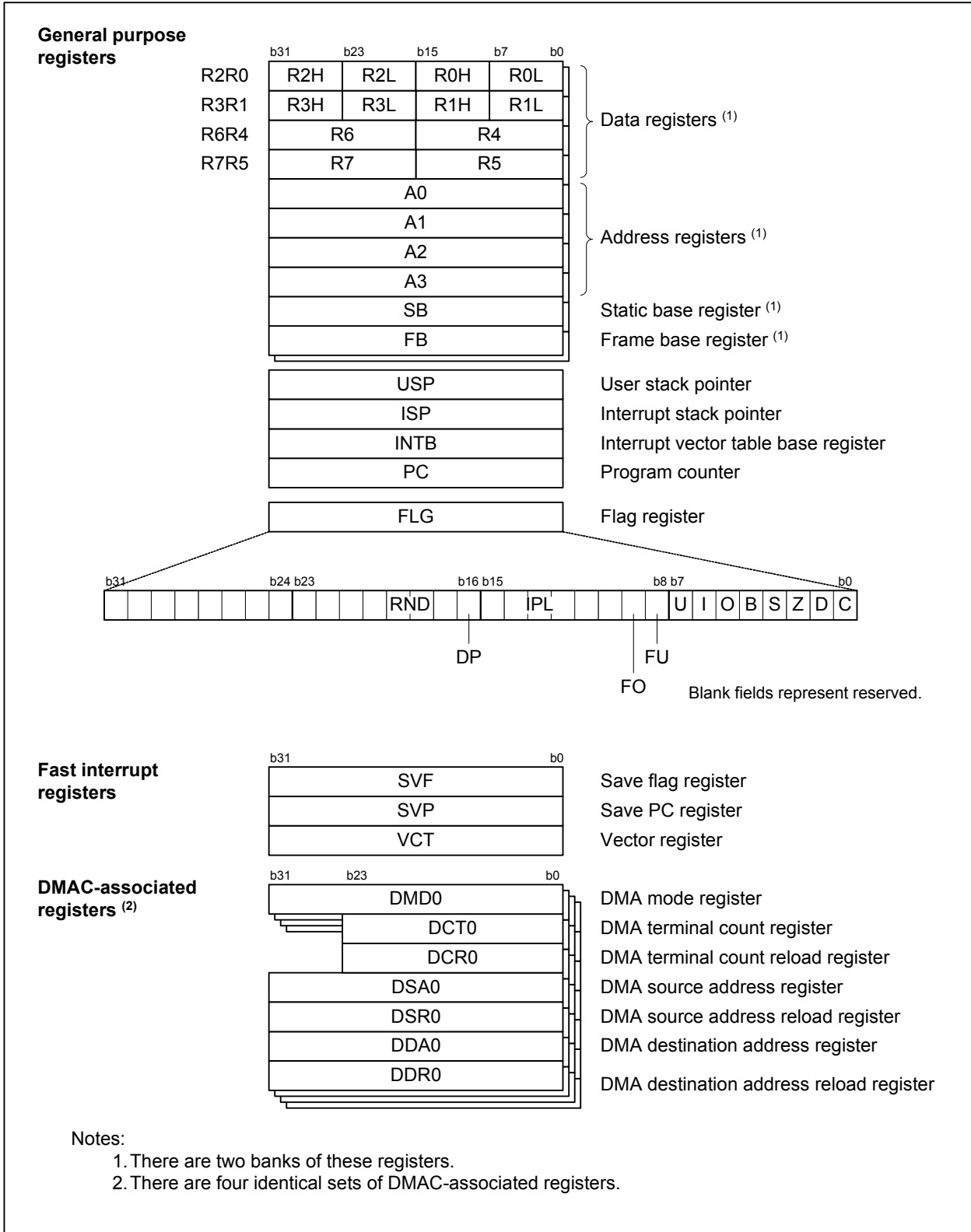


Figure 2.1 CPU Registers

2.1 General Purpose Registers

2.1.1 Data Registers (R2R0, R3R1, R6R4, and R7R5)

These 32-bit registers are primarily used for transfers and arithmetic/logic operations.

Each of the registers can be divided into upper and lower 16-bit registers, e.g. R2R0 can be divided into R2 and R0, R3R0 can be divided into R3 and R1, etc.

Moreover, data registers R2R0 and R3R1 can be divided into four 8-bit data registers: upper (R2H and R3H), mid-upper (R2L and R3L), mid-lower (R0H and R1H), and lower (R0L and R1L).

2.1.2 Address Registers (A0, A1, A2, and A3)

These 32-bit registers have functions similar to data registers. They are also used for address register indirect addressing and address register relative addressing.

2.1.3 Static Base Register (SB)

This 32-bit register is used for SB relative addressing.

2.1.4 Frame Base Register (FB)

This 32-bit register is used for FB relative addressing.

2.1.5 Program Counter (PC)

This 32-bit counter indicates the address of the instruction to be executed next.

2.1.6 Interrupt Vector Table Base Register (INTB)

This 32-bit register indicates the start address of a relocatable vector table.

2.1.7 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Two types of 32-bit stack pointers (SPs) are provided: user stack pointer (USP) and interrupt stack pointer (ISP).

Use the stack pointer select flag (U flag) to select either the user stack pointer (USP) or the interrupt stack pointer (ISP). The U flag is bit 7 in the flag register (FLG). Refer to 2.1.8 "Flag Register (FLG)" for details.

To minimize the overhead of interrupt sequence due to less memory access, set the user stack pointer (USP) or the interrupt stack pointer (ISP) to a multiple of 4.

2.1.8 Flag Register (FLG)

This 32-bit register indicates the CPU status.

2.1.8.1 Carry Flag (C flag)

This flag becomes 1 when any of the carry, borrow, shifted-out bit, etc. is generated in the arithmetic logic unit (ALU).

2.1.8.2 Debug Flag (D flag)

This flag is only for debugging. Only set this bit to 0.

2.1.8.3 Zero Flag (Z flag)

This flag becomes 1 when the result of an operation is 0; otherwise it is 0.

2.1.8.4 Sign Flag (S flag)

This flag becomes 1 when the result of an operation is a negative value; otherwise it is 0.

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when the register bank 0 is selected, and 1 when the register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 if an overflow occurs in an operation; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.

It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand has invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand has invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of three bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is acceptable when the interrupt request level is higher than the selected IPL.

When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to take. It is used in the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt is generated.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt is generated.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt is generated.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate, etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set DMA transfer counting.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded value for DMA source address register.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination address.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

3. Memory

Figure 3.1 shows the memory map of the R32C/118A Group.

The R32C/118A Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

The internal ROM is mapped to the end of the memory map with the ending address fixed at FFFFFFFFh. Therefore, the 1-Mbyte internal ROM is mapped from FFF00000h to FFFFFFFFh.

The fixed interrupt vector table which contains each start address of interrupt handlers is mapped from FFFFFFFDCh to FFFFFFFFh.

The internal RAM is mapped to the beginning of the memory map with the starting address fixed at 00000400h. Therefore, the 96-Kbyte internal RAM is mapped from 00000400h to 000183FFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutines and/or interrupt handlers.

Special Function Registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved. No access is allowed.

In memory expansion mode or microprocessor mode, some spaces are reserved for internal use and should not be accessed.

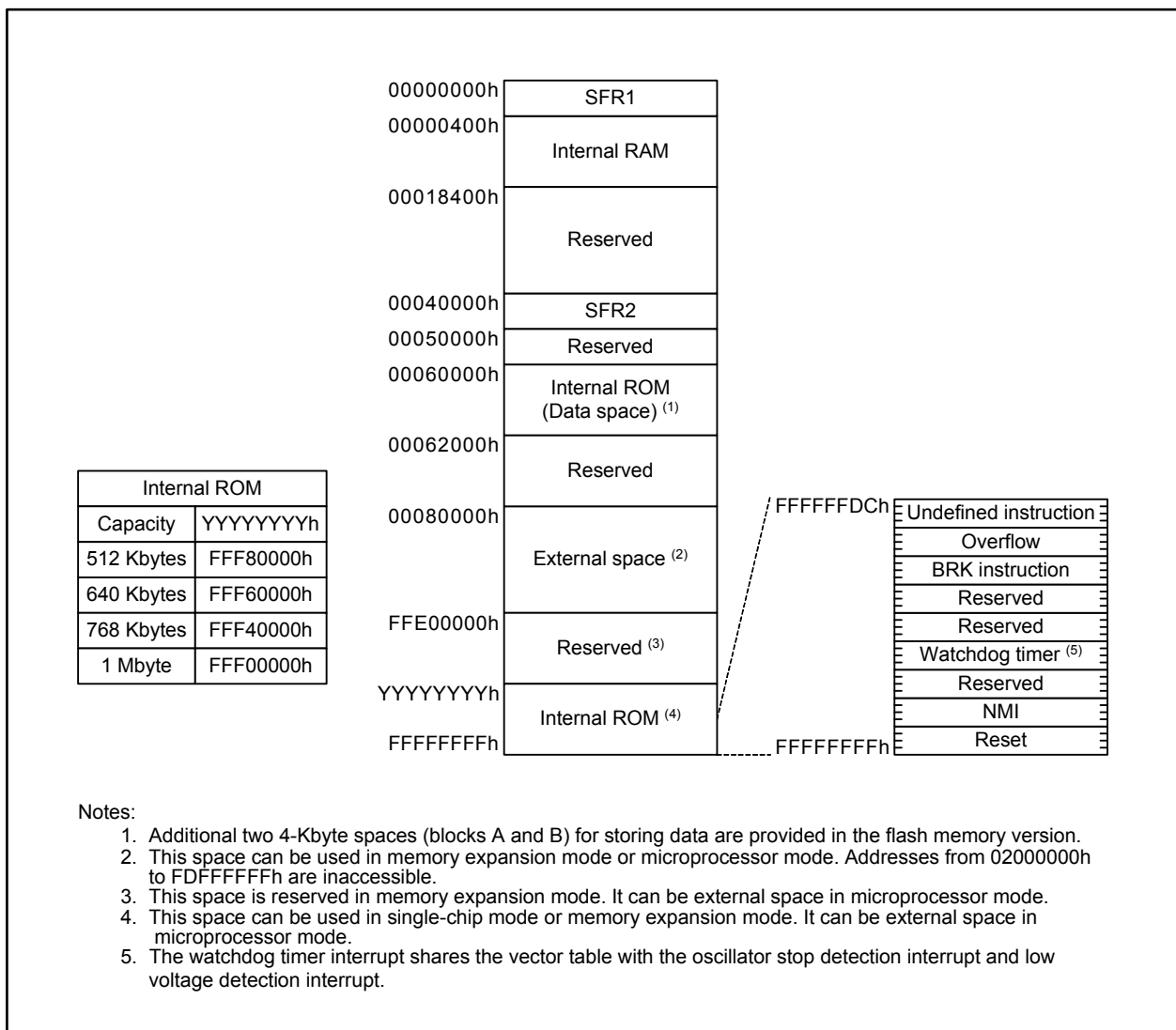


Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.55 SFR List (55) list the SFR details.

Table 4.1 SFR List (1)

| Address | Register | Symbol | Reset Value |
|-----------------------|--|--------|-------------|
| 000000h | | | |
| 000001h | | | |
| 000002h | | | |
| 000003h | | | |
| 000004h | Clock Control Register | CCR | 0001 1000b |
| 000005h | | | |
| 000006h | Flash Memory Control Register | FMCR | 0000 0001b |
| 000007h | Protect Release Register | PRR | 00h |
| 000008h | Flash Memory Rewrite Bus Control Register | FEBC | 0000h |
| 000009h | | | |
| 00000Ah | | | |
| 00000Bh | | | |
| 00000Ch | | | |
| 00000Dh | | | |
| 00000Eh | | | |
| 00000Fh | | | |
| 000010h | External Bus Control Register 3 | EBC3 | 0000h |
| 000011h | | | |
| 000012h | Chip Selects 2 and 3 Boundary Setting Register | CB23 | 00h |
| 000013h | | | |
| 000014h | External Bus Control Register 2 | EBC2 | 0000h |
| 000015h | | | |
| 000016h | Chip Selects 1 and 2 Boundary Setting Register | CB12 | 00h |
| 000017h | | | |
| 000018h | External Bus Control Register 1 | EBC1 | 0000h |
| 000019h | | | |
| 00001Ah | Chip selects 0 and 1 Boundary Setting Register | CB01 | 00h |
| 00001Bh | | | |
| 00001Ch | External Bus Control Register 0 | EBC0 | 0000h |
| 00001Dh | | | |
| 00001Eh | Peripheral Bus Control Register | PBC | 0504h |
| 00001Fh | | | |
| 000020h to 00005Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.2 SFR List (2)

| Address | Register | Symbol | Reset Value |
|---------|---|---------------|-------------|
| 000060h | | | |
| 000061h | Timer B5 Interrupt Control Register | TB5IC | XXXX X000b |
| 000062h | UART5 Transmit/NACK Interrupt Control Register | S5TIC | XXXX X000b |
| 000063h | UART2 Receive/ACK Interrupt Control Register/I ² C Bus Line Interrupt Control Register | S2RIC/I2CLIC | XXXX X000b |
| 000064h | UART6 Transmit/NACK Interrupt Control Register | S6TIC | XXXX X000b |
| 000065h | UART3 Receive/ACK Interrupt Control Register | S3RIC | XXXX X000b |
| 000066h | UART5/6 Bus Collision, Start Condition/Stop Condition Detection Interrupt Control Register | BCN5IC/BCN6IC | XXXX X000b |
| 000067h | UART4 Receive/ACK Interrupt Control Register | S4RIC | XXXX X000b |
| 000068h | DMA0 Transfer Complete Interrupt Control Register | DM0IC | XXXX X000b |
| 000069h | UART0/3 Bus Collision, Start Condition/Stop Condition Detection Interrupt Control Register | BCN0IC/BCN3IC | XXXX X000b |
| 00006Ah | DMA2 Transfer Complete Interrupt Control Register | DM2IC | XXXX X000b |
| 00006Bh | A/D Converter 0 Convert Completion Interrupt Control Register | AD0IC | XXXX X000b |
| 00006Ch | Timer A0 Interrupt Control Register | TA0IC | XXXX X000b |
| 00006Dh | Intelligent I/O Interrupt Control Register 0 | IIO0IC | XXXX X000b |
| 00006Eh | Timer A2 Interrupt Control Register | TA2IC | XXXX X000b |
| 00006Fh | Intelligent I/O Interrupt Control Register 2 | IIO2IC | XXXX X000b |
| 000070h | Timer A4 Interrupt Control Register | TA4IC | XXXX X000b |
| 000071h | Intelligent I/O Interrupt Control Register 4 | IIO4IC | XXXX X000b |
| 000072h | UART0 Receive/ACK Interrupt Control Register | S0RIC | XXXX X000b |
| 000073h | Intelligent I/O Interrupt Control Register 6 | IIO6IC | XXXX X000b |
| 000074h | UART1 Receive/ACK Interrupt Control Register | S1RIC | XXXX X000b |
| 000075h | Intelligent I/O Interrupt Control Register 8 | IIO8IC | XXXX X000b |
| 000076h | Timer B1 Interrupt Control Register | TB1IC | XXXX X000b |
| 000077h | Intelligent I/O Interrupt Control Register 10 | IIO10IC | XXXX X000b |
| 000078h | Timer B3 Interrupt Control Register | TB3IC | XXXX X000b |
| 000079h | | | |
| 00007Ah | INT5 Interrupt Control Register | INT5IC | XX00 X000b |
| 00007Bh | CAN0 Wake-up Interrupt Control Register | C0WIC | XXXX X000b |
| 00007Ch | INT3 Interrupt Control Register | INT3IC | XX00 X000b |
| 00007Dh | | | |
| 00007Eh | INT1 Interrupt Control Register | INT1IC | XX00 X000b |
| 00007Fh | | | |
| 000080h | | | |
| 000081h | UART2 Transmit/NACK Interrupt Control Register/I ² C-Bus Interrupt Control Register | S2TIC/I2CIC | XXXX X000b |
| 000082h | UART5 Receive/ACK Interrupt Control Register | S5RIC | XXXX X000b |
| 000083h | UART3 Transmit/NACK Interrupt Control Register | S3TIC | XXXX X000b |
| 000084h | UART6 Receive/ACK Interrupt Control Register | S6RIC | XXXX X000b |
| 000085h | UART4 Transmit/NACK Interrupt Control Register | S4TIC | XXXX X000b |
| 000086h | | | |
| 000087h | UART2 Bus Collision, Start Condition/Stop Condition Detection Interrupt Control Register | BCN2IC | XXXX X000b |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.3 SFR List (3)

| Address | Register | Symbol | Reset Value |
|---------|--|---------------|-------------|
| 000088h | DMA1 Transfer Complete Interrupt Control Register | DM1IC | XXXX X000b |
| 000089h | UART1/4 Bus Collision, Start Condition/Stop Condition Detection Interrupt Control Register | BCN1IC/BCN4IC | XXXX X000b |
| 00008Ah | DMA3 Transfer Complete Interrupt Control Register | DM3IC | XXXX X000b |
| 00008Bh | Key Input Interrupt Control Register | KUPIC | XXXX X000b |
| 00008Ch | Timer A1 Interrupt Control Register | TA1IC | XXXX X000b |
| 00008Dh | Intelligent I/O Interrupt Control Register 1 | IIO1IC | XXXX X000b |
| 00008Eh | Timer A3 Interrupt Control Register | TA3IC | XXXX X000b |
| 00008Fh | Intelligent I/O Interrupt Control Register 3 | IIO3IC | XXXX X000b |
| 000090h | UART0 Transmit/NACK Interrupt Control Register | S0TIC | XXXX X000b |
| 000091h | Intelligent I/O Interrupt Control Register 5 | IIO5IC | XXXX X000b |
| 000092h | UART1 Transmit/NACK Interrupt Control Register | S1TIC | XXXX X000b |
| 000093h | Intelligent I/O Interrupt Control Register 7 | IIO7IC | XXXX X000b |
| 000094h | Timer B0 Interrupt Control Register | TB0IC | XXXX X000b |
| 000095h | Intelligent I/O Interrupt Control Register 9 | IIO9IC | XXXX X000b |
| 000096h | Timer B2 Interrupt Control Register | TB2IC | XXXX X000b |
| 000097h | Intelligent I/O Interrupt Control Register 11 | IIO11IC | XXXX X000b |
| 000098h | Timer B4 Interrupt Control Register | TB4IC | XXXX X000b |
| 000099h | | | |
| 00009Ah | INT4 Interrupt Control Register | INT4IC | XX00 X000b |
| 00009Bh | CAN1 Wake-up Interrupt Control Register | C1WIC | XXXX X000b |
| 00009Ch | INT2 Interrupt Control Register | INT2IC | XX00 X000b |
| 00009Dh | | | |
| 00009Eh | INT0 Interrupt Control Register | INT0IC | XX00 X000b |
| 00009Fh | | | |
| 0000A0h | Intelligent I/O Interrupt Request Register 0 | IIO0IR | 0000 0XX1b |
| 0000A1h | Intelligent I/O Interrupt Request Register 1 | IIO1IR | 0000 0XX1b |
| 0000A2h | Intelligent I/O Interrupt Request Register 2 | IIO2IR | 0000 0X01b |
| 0000A3h | Intelligent I/O Interrupt Request Register 3 | IIO3IR | 0000 XXX1b |
| 0000A4h | Intelligent I/O Interrupt Request Register 4 | IIO4IR | 000X 0XX1b |
| 0000A5h | Intelligent I/O Interrupt Request Register 5 | IIO5IR | 000X 0XX1b |
| 0000A6h | Intelligent I/O Interrupt Request Register 6 | IIO6IR | 000X 0XX1b |
| 0000A7h | Intelligent I/O Interrupt Request Register 7 | IIO7IR | X00X 0XX1b |
| 0000A8h | Intelligent I/O Interrupt Request Register 8 | IIO8IR | XX0X 0XX1b |
| 0000A9h | Intelligent I/O Interrupt Request Register 9 | IIO9IR | 0X00 0XX1b |
| 0000AAh | Intelligent I/O Interrupt Request Register 10 | IIO10IR | 0X00 0XX1b |
| 0000ABh | Intelligent I/O Interrupt Request Register 11 | IIO11IR | 0X00 0XX1b |
| 0000ACh | | | |
| 0000ADh | | | |
| 0000AEh | | | |
| 0000AFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.4 SFR List (4)

| Address | Register | Symbol | Reset Value |
|---------|---|---------|-------------|
| 0000B0h | Intelligent I/O Interrupt Enable Register 0 | IIO0IE | 00h |
| 0000B1h | Intelligent I/O Interrupt Enable Register 1 | IIO1IE | 00h |
| 0000B2h | Intelligent I/O Interrupt Enable Register 2 | IIO2IE | 00h |
| 0000B3h | Intelligent I/O Interrupt Enable Register 3 | IIO3IE | 00h |
| 0000B4h | Intelligent I/O Interrupt Enable Register 4 | IIO4IE | 00h |
| 0000B5h | Intelligent I/O Interrupt Enable Register 5 | IIO5IE | 00h |
| 0000B6h | Intelligent I/O Interrupt Enable Register 6 | IIO6IE | 00h |
| 0000B7h | Intelligent I/O Interrupt Enable Register 7 | IIO7IE | 00h |
| 0000B8h | Intelligent I/O Interrupt Enable Register 8 | IIO8IE | 00h |
| 0000B9h | Intelligent I/O Interrupt Enable Register 9 | IIO9IE | 00h |
| 0000BAh | Intelligent I/O Interrupt Enable Register 10 | IIO10IE | 00h |
| 0000BBh | Intelligent I/O Interrupt Enable Register 11 | IIO11IE | 00h |
| 0000BCh | | | |
| 0000BDh | | | |
| 0000BEh | | | |
| 0000BFh | | | |
| 0000C0h | | | |
| 0000C1h | CAN0 Transmit Interrupt Control Register | C0TIC | XXXX X000b |
| 0000C2h | | | |
| 0000C3h | CAN0 Error Interrupt Control Register | C0EIC | XXXX X000b |
| 0000C4h | | | |
| 0000C5h | CAN1 Receive Interrupt Control Register | C1RIC | XXXX X000b |
| 0000C6h | | | |
| 0000C7h | | | |
| 0000C8h | | | |
| 0000C9h | | | |
| 0000CAh | | | |
| 0000CBh | | | |
| 0000CCh | | | |
| 0000CDh | | | |
| 0000CEh | | | |
| 0000CFh | | | |
| 0000D0h | CAN0 Transmit FIFO Interrupt Control Register | C0FTIC | XXXX X000b |
| 0000D1h | | | |
| 0000D2h | CAN1 Transmit FIFO Interrupt Control Register | C1FTIC | XXXX X000b |
| 0000D3h | | | |
| 0000D4h | | | |
| 0000D5h | | | |
| 0000D6h | | | |
| 0000D7h | | | |
| 0000D8h | | | |
| 0000D9h | UART9 Transmit Interrupt Control Register | S9TIC | XXXX X000b |
| 0000DAh | | | |
| 0000DBh | UART10 Transmit Interrupt Control Register | S10TIC | XXXX X000b |
| 0000DCh | | | |
| 0000DDh | UART7 Transmit Interrupt Control Register | S7TIC | XXXX X000b |
| 0000DEh | INT7 Interrupt Control Register | INT7IC | XX00 X000b |
| 0000DFh | UART8 Transmit Interrupt Control Register | S8TIC | XXXX X000b |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.5 SFR List (5)

| Address | Register | Symbol | Reset Value |
|---------|---|-------------|-------------|
| 0000E0h | | | |
| 0000E1h | CAN0 Receive Interrupt Control Register | C0RIC | XXXX X000b |
| 0000E2h | | | |
| 0000E3h | CAN1 Transmit Interrupt Control Register | C1TIC | XXXX X000b |
| 0000E4h | | | |
| 0000E5h | CAN1 Error Interrupt Control Register | C1EIC | XXXX X000b |
| 0000E6h | | | |
| 0000E7h | | | |
| 0000E8h | | | |
| 0000E9h | | | |
| 0000EAh | | | |
| 0000EBh | | | |
| 0000ECh | | | |
| 0000EDh | | | |
| 0000EEh | | | |
| 0000EFh | | | |
| 0000F0h | CAN0 Receive FIFO Interrupt Control Register | C0FRIC | XXXX X000b |
| 0000F1h | | | |
| 0000F2h | CAN1 Receive FIFO Interrupt Control Register | C1FRIC | XXXX X000b |
| 0000F3h | | | |
| 0000F4h | | | |
| 0000F5h | | | |
| 0000F6h | | | |
| 0000F7h | | | |
| 0000F8h | | | |
| 0000F9h | UART9 Receive Interrupt Control Register | S9RIC | XXXX X000b |
| 000FAh | | | |
| 000FBh | UART10 Receive Interrupt Control Register | S10RIC | XXXX X000b |
| 000FCh | INT8 Interrupt Control Register | INT8IC | XX00 X000b |
| 000FDh | UART7 Receive Interrupt Control Register | S7RIC | XXXX X000b |
| 000FEh | INT6 Interrupt Control Register | INT6IC | XX00 X000b |
| 000FFh | UART8 Receive Interrupt Control Register | S8RIC | XXXX X000b |
| 000100h | Group 1 Time Measurement/Waveform Generation Register 0 | G1TM0/G1PO0 | XXXXh |
| 000101h | | | |
| 000102h | Group 1 Time Measurement/Waveform Generation Register 1 | G1TM1/G1PO1 | XXXXh |
| 000103h | | | |
| 000104h | Group 1 Time Measurement/Waveform Generation Register 2 | G1TM2/G1PO2 | XXXXh |
| 000105h | | | |
| 000106h | Group 1 Time Measurement/Waveform Generation Register 3 | G1TM3/G1PO3 | XXXXh |
| 000107h | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.6 SFR List (6)

| Address | Register | Symbol | Reset Value |
|-----------------------|---|-------------|-------------|
| 000108h | Group 1 Time Measurement/Waveform Generation Register 4 | G1TM4/G1PO4 | XXXXh |
| 000109h | | | |
| 00010Ah | Group 1 Time Measurement/Waveform Generation Register 5 | G1TM5/G1PO5 | XXXXh |
| 00010Bh | | | |
| 00010Ch | Group 1 Time Measurement/Waveform Generation Register 6 | G1TM6/G1PO6 | XXXXh |
| 00010Dh | | | |
| 00010Eh | Group 1 Time Measurement/Waveform Generation Register 7 | G1TM7/G1PO7 | XXXXh |
| 00010Fh | | | |
| 000110h | Group 1 Waveform Generation Control Register 0 | G1POCR0 | 0000 X000b |
| 000111h | Group 1 Waveform Generation Control Register 1 | G1POCR1 | 0X00 X000b |
| 000112h | Group 1 Waveform Generation Control Register 2 | G1POCR2 | 0X00 X000b |
| 000113h | Group 1 Waveform Generation Control Register 3 | G1POCR3 | 0X00 X000b |
| 000114h | Group 1 Waveform Generation Control Register 4 | G1POCR4 | 0X00 X000b |
| 000115h | Group 1 Waveform Generation Control Register 5 | G1POCR5 | 0X00 X000b |
| 000116h | Group 1 Waveform Generation Control Register 6 | G1POCR6 | 0X00 X000b |
| 000117h | Group 1 Waveform Generation Control Register 7 | G1POCR7 | 0X00 X000b |
| 000118h | Group 1 Time Measurement Control Register 0 | G1TMCR0 | 00h |
| 000119h | Group 1 Time Measurement Control Register 1 | G1TMCR1 | 00h |
| 00011Ah | Group 1 Time Measurement Control Register 2 | G1TMCR2 | 00h |
| 00011Bh | Group 1 Time Measurement Control Register 3 | G1TMCR3 | 00h |
| 00011Ch | Group 1 Time Measurement Control Register 4 | G1TMCR4 | 00h |
| 00011Dh | Group 1 Time Measurement Control Register 5 | G1TMCR5 | 00h |
| 00011Eh | Group 1 Time Measurement Control Register 6 | G1TMCR6 | 00h |
| 00011Fh | Group 1 Time Measurement Control Register 7 | G1TMCR7 | 00h |
| 000120h | Group 1 Base Timer Register | G1BT | XXXXh |
| 000121h | | | |
| 000122h | Group 1 Base Timer Control Register 0 | G1BCR0 | 00h |
| 000123h | Group 1 Base Timer Control Register 1 | G1BCR1 | 0000 0000b |
| 000124h | Group 1 Time Measurement Prescaler Register 6 | G1TPR6 | 00h |
| 000125h | Group 1 Time Measurement Prescaler Register 7 | G1TPR7 | 00h |
| 000126h | Group 1 Function Enable Register | G1FE | 00h |
| 000127h | Group 1 Function Select Register | G1FS | 00h |
| 000128h | | | |
| 000129h | | | |
| 00012Ah | | | |
| 00012Bh | | | |
| 00012Ch | | | |
| 00012Dh | | | |
| 00012Eh | | | |
| 00012Fh | | | |
| 000130h to 00013Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.7 SFR List (7)

| Address | Register | Symbol | Reset Value |
|---------|--|---------|-------------|
| 000140h | Group 2 Waveform Generation Register 0 | G2PO0 | XXXXh |
| 000141h | | | |
| 000142h | Group 2 Waveform Generation Register 1 | G2PO1 | XXXXh |
| 000143h | | | |
| 000144h | Group 2 Waveform Generation Register 2 | G2PO2 | XXXXh |
| 000145h | | | |
| 000146h | Group 2 Waveform Generation Register 3 | G2PO3 | XXXXh |
| 000147h | | | |
| 000148h | Group 2 Waveform Generation Register 4 | G2PO4 | XXXXh |
| 000149h | | | |
| 00014Ah | Group 2 Waveform Generation Register 5 | G2PO5 | XXXXh |
| 00014Bh | | | |
| 00014Ch | Group 2 Waveform Generation Register 6 | G2PO6 | XXXXh |
| 00014Dh | | | |
| 00014Eh | Group 2 Waveform Generation Register 7 | G2PO7 | XXXXh |
| 00014Fh | | | |
| 000150h | Group 2 Waveform Generation Control Register 0 | G2POCR0 | 0000 0000b |
| 000151h | Group 2 Waveform Generation Control Register 1 | G2POCR1 | 0000 0000b |
| 000152h | Group 2 Waveform Generation Control Register 2 | G2POCR2 | 0000 0000b |
| 000153h | Group 2 Waveform Generation Control Register 3 | G2POCR3 | 0000 0000b |
| 000154h | Group 2 Waveform Generation Control Register 4 | G2POCR4 | 0000 0000b |
| 000155h | Group 2 Waveform Generation Control Register 5 | G2POCR5 | 0000 0000b |
| 000156h | Group 2 Waveform Generation Control Register 6 | G2POCR6 | 0000 0000b |
| 000157h | Group 2 Waveform Generation Control Register 7 | G2POCR7 | 0000 0000b |
| 000158h | | | |
| 000159h | | | |
| 00015Ah | | | |
| 00015Bh | | | |
| 00015Ch | | | |
| 00015Dh | | | |
| 00015Eh | | | |
| 00015Fh | | | |
| 000160h | Group 2 Base Timer Register | G2BT | XXXXh |
| 000161h | | | |
| 000162h | Group 2 Base Timer Control Register 0 | G2BCR0 | 00h |
| 000163h | Group 2 Base Timer Control Register 1 | G2BCR1 | 0000 0000b |
| 000164h | Base Timer Start Register | BTSR | XXXX 0000b |
| 000165h | | | |
| 000166h | Group 2 Function Enable Register | G2FE | 00h |
| 000167h | Group 2 RTP Output Buffer Register | G2RTP | 00h |
| 000168h | | | |
| 000169h | | | |
| 00016Ah | Group 2 Serial Interface Mode Register | G2MR | 00XX X000b |
| 00016Bh | Group 2 Serial Interface Control Register | G2CR | 0000 X110b |
| 00016Ch | Group 2 SI/O Transmit Buffer Register | G2TB | XXXXh |
| 00016Dh | | | |
| 00016Eh | Group 2 SI/O Receive Buffer Register | G2RB | XXXXh |
| 00016Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.8 SFR List (8)

| Address | Register | Symbol | Reset Value |
|---------|---|-------------|-------------|
| 000170h | Group 2 IEBus Address Register | IEAR | XXXXh |
| 000171h | | | |
| 000172h | Group 2 IEBus Control Register | IECR | 00XX X000b |
| 000173h | Group 2 IEBus Transmit Interrupt Source Detect Register | IETIF | XXX0 0000b |
| 000174h | Group 2 IEBus Receive Interrupt Source Detect Register | IERIF | XXX0 0000b |
| 000175h | | | |
| 000176h | | | |
| 000177h | | | |
| 000178h | | | |
| 000179h | | | |
| 00017Ah | | | |
| 00017Bh | | | |
| 00017Ch | | | |
| 00017Dh | | | |
| 00017Eh | | | |
| 00017Fh | | | |
| 000180h | Group 0 Time Measurement/Waveform Generation Register 0 | G0TM0/G0PO0 | XXXXh |
| 000181h | | | |
| 000182h | Group 0 Time Measurement/Waveform Generation Register 1 | G0TM1/G0PO1 | XXXXh |
| 000183h | | | |
| 000184h | Group 0 Time Measurement/Waveform Generation Register 2 | G0TM2/G0PO2 | XXXXh |
| 000185h | | | |
| 000186h | Group 0 Time Measurement/Waveform Generation Register 3 | G0TM3/G0PO3 | XXXXh |
| 000187h | | | |
| 000188h | Group 0 Time Measurement/Waveform Generation Register 4 | G0TM4/G0PO4 | XXXXh |
| 000189h | | | |
| 00018Ah | Group 0 Time Measurement/Waveform Generation Register 5 | G0TM5/G0PO5 | XXXXh |
| 00018Bh | | | |
| 00018Ch | Group 0 Time Measurement/Waveform Generation Register 6 | G0TM6/G0PO6 | XXXXh |
| 00018Dh | | | |
| 00018Eh | Group 0 Time Measurement/Waveform Generation Register 7 | G0TM7/G0PO7 | XXXXh |
| 00018Fh | | | |
| 000190h | Group 0 Waveform Generation Control Register 0 | G0POCR0 | 0000 X000b |
| 000191h | Group 0 Waveform Generation Control Register 1 | G0POCR1 | 0X00 X000b |
| 000192h | Group 0 Waveform Generation Control Register 2 | G0POCR2 | 0X00 X000b |
| 000193h | Group 0 Waveform Generation Control Register 3 | G0POCR3 | 0X00 X000b |
| 000194h | Group 0 Waveform Generation Control Register 4 | G0POCR4 | 0X00 X000b |
| 000195h | Group 0 Waveform Generation Control Register 5 | G0POCR5 | 0X00 X000b |
| 000196h | Group 0 Waveform Generation Control Register 6 | G0POCR6 | 0X00 X000b |
| 000197h | Group 0 Waveform Generation Control Register 7 | G0POCR7 | 0X00 X000b |
| 000198h | Group 0 Time Measurement Control Register 0 | G0TMCR0 | 00h |
| 000199h | Group 0 Time Measurement Control Register 1 | G0TMCR1 | 00h |
| 00019Ah | Group 0 Time Measurement Control Register 2 | G0TMCR2 | 00h |
| 00019Bh | Group 0 Time Measurement Control Register 3 | G0TMCR3 | 00h |
| 00019Ch | Group 0 Time Measurement Control Register 4 | G0TMCR4 | 00h |
| 00019Dh | Group 0 Time Measurement Control Register 5 | G0TMCR5 | 00h |
| 00019Eh | Group 0 Time Measurement Control Register 6 | G0TMCR6 | 00h |
| 00019Fh | Group 0 Time Measurement Control Register 7 | G0TMCR7 | 00h |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

| Address | Register | Symbol | Reset Value |
|---------|---|--------|-------------|
| 0001A0h | Group 0 Base Timer Register | G0BT | XXXXh |
| 0001A1h | | | |
| 0001A2h | Group 0 Base Timer Control Register 0 | G0BCR0 | 00h |
| 0001A3h | Group 0 Base Timer Control Register 1 | G0BCR1 | 0000 0000b |
| 0001A4h | Group 0 Time Measurement Prescaler Register 6 | G0TPR6 | 00h |
| 0001A5h | Group 0 Time Measurement Prescaler Register 7 | G0TPR7 | 00h |
| 0001A6h | Group 0 Function Enable Register | G0FE | 00h |
| 0001A7h | Group 0 Function Select Register | G0FS | 00h |
| 0001A8h | | | |
| 0001A9h | | | |
| 0001AAh | | | |
| 0001ABh | | | |
| 0001ACh | | | |
| 0001ADh | | | |
| 0001AEh | | | |
| 0001AFh | | | |
| 0001B0h | | | |
| 0001B1h | | | |
| 0001B2h | | | |
| 0001B3h | | | |
| 0001B4h | | | |
| 0001B5h | | | |
| 0001B6h | | | |
| 0001B7h | | | |
| 0001B8h | | | |
| 0001B9h | | | |
| 0001BAh | | | |
| 0001BBh | | | |
| 0001BCh | | | |
| 0001BDh | | | |
| 0001BEh | | | |
| 0001BFh | | | |
| 0001C0h | | | |
| 0001C1h | | | |
| 0001C2h | | | |
| 0001C3h | | | |
| 0001C4h | UART5 Special Mode Register 4 | U5SMR4 | 00h |
| 0001C5h | UART5 Special Mode Register 3 | U5SMR3 | 00h |
| 0001C6h | UART5 Special Mode Register 2 | U5SMR2 | 00h |
| 0001C7h | UART5 Special Mode Register | U5SMR | 00h |
| 0001C8h | UART5 Transmit/Receive Mode Register | U5MR | 00h |
| 0001C9h | UART5 Bit Rate Register | U5BRG | XXh |
| 0001CAh | UART5 Transmit Buffer Register | U5TB | XXXXh |
| 0001CBh | | | |
| 0001CCh | UART5 Transmit/Receive Control Register 0 | U5C0 | 0000 1000b |
| 0001CDh | UART5 Transmit/Receive Control Register 1 | U5C1 | 0000 0010b |
| 0001CEh | UART5 Receive Buffer Register | U5RB | XXXXh |
| 0001CFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.10 SFR List (10)

| Address | Register | Symbol | Reset Value |
|---------|--|--------|-------------|
| 0001D0h | | | |
| 0001D1h | | | |
| 0001D2h | | | |
| 0001D3h | | | |
| 0001D4h | UART6 Special Mode Register 4 | U6SMR4 | 00h |
| 0001D5h | UART6 Special Mode Register 3 | U6SMR3 | 00h |
| 0001D6h | UART6 Special Mode Register 2 | U6SMR2 | 00h |
| 0001D7h | UART6 Special Mode Register | U6SMR | 00h |
| 0001D8h | UART6 Transmit/Receive Mode Register | U6MR | 00h |
| 0001D9h | UART6 Bit Rate Register | U6BRG | XXh |
| 0001DAh | UART6 Transmit Buffer Register | U6TB | XXXXh |
| 0001DBh | | | |
| 0001DCh | UART6 Transmit/Receive Control Register 0 | U6C0 | 0000 1000b |
| 0001DDh | UART6 Transmit/Receive Control Register 1 | U6C1 | 0000 0010b |
| 0001DEh | UART6 Receive Buffer Register | U6RB | XXXXh |
| 0001DFh | | | |
| 0001E0h | UART7 Transmit/Receive Mode Register | U7MR | 00h |
| 0001E1h | UART7 Bit Rate Register | U7BRG | XXh |
| 0001E2h | UART7 Transmit Buffer Register | U7TB | XXXXh |
| 0001E3h | | | |
| 0001E4h | UART7 Transmit/Receive Control Register 0 | U7C0 | 00X0 1000b |
| 0001E5h | UART7 Transmit/Receive Control Register 1 | U7C1 | XXXX 0010b |
| 0001E6h | UART7 Receive Buffer Register | U7RB | XXXXh |
| 0001E7h | | | |
| 0001E8h | UART8 Transmit/Receive Mode Register | U8MR | 00h |
| 0001E9h | UART8 Bit Rate Register | U8BRG | XXh |
| 0001EAh | UART8 Transmit Buffer Register | U8TB | XXXXh |
| 0001EBh | | | |
| 0001ECh | UART8 Transmit/Receive Control Register 0 | U8C0 | 00X0 1000b |
| 0001EDh | UART8 Transmit/Receive Control Register 1 | U8C1 | XXXX 0010b |
| 0001EEh | UART8 Receive Buffer Register | U8RB | XXXXh |
| 0001EFh | | | |
| 0001F0h | UART7, UART8 Transmit/Receive Control Register 2 | U78CON | X000 0000b |
| 0001F1h | | | |
| 0001F2h | | | |
| 0001F3h | | | |
| 0001F4h | | | |
| 0001F5h | | | |
| 0001F6h | | | |
| 0001F7h | | | |
| 0001F8h | | | |
| 0001F9h | | | |
| 0001FAh | | | |
| 0001FBh | | | |
| 0001FCh | | | |
| 0001FDh | | | |
| 0001FEh | | | |
| 0001FFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.11 SFR List (11)

| Address | Register | Symbol | Reset Value |
|-----------------------|---|-----------|-------------|
| 000200h to 0002BFh | | | |
| 0002C0h 0002C1h | X0 Register/Y0 Register | X0R/Y0R | XXXXh |
| 0002C2h 0002C3h | X1 Register/Y1 Register | X1R/Y1R | XXXXh |
| 0002C4h 0002C5h | X2 Register/Y2 Register | X2R/Y2R | XXXXh |
| 0002C6h 0002C7h | X3 Register/Y3 Register | X3R/Y3R | XXXXh |
| 0002C8h 0002C9h | X4 Register/Y4 Register | X4R/Y4R | XXXXh |
| 0002CAh 0002CBh | X5 Register/Y5 Register | X5R/Y5R | XXXXh |
| 0002CCh 0002CDh | X6 Register/Y6 Register | X6R/Y6R | XXXXh |
| 0002CEh 0002CFh | X7 Register/Y7 Register | X7R/Y7R | XXXXh |
| 0002D0h 0002D1h | X8 Register/Y8 Register | X8R/Y8R | XXXXh |
| 0002D2h 0002D3h | X9 Register/Y9 Register | X9R/Y9R | XXXXh |
| 0002D4h 0002D5h | X10 Register/Y10 Register | X10R/Y10R | XXXXh |
| 0002D6h 0002D7h | X11 Register/Y11 Register | X11R/Y11R | XXXXh |
| 0002D8h 0002D9h | X12 Register/Y12 Register | X12R/Y12R | XXXXh |
| 0002DAh 0002DBh | X13 Register/Y13 Register | X13R/Y13R | XXXXh |
| 0002DCh 0002DDh | X14 Register/Y14 Register | X14R/Y14R | XXXXh |
| 0002DEh 0002DFh | X15 Register/Y15 Register | X15R/Y15R | XXXXh |
| 0002E0h 0002E1h | X-Y Control Register | XYC | XXXX XX00b |
| 0002E2h 0002E3h | | | |
| 0002E4h | UART1 Special Mode Register 4 | U1SMR4 | 00h |
| 0002E5h | UART1 Special Mode Register 3 | U1SMR3 | 00h |
| 0002E6h | UART1 Special Mode Register 2 | U1SMR2 | 00h |
| 0002E7h | UART1 Special Mode Register | U1SMR | 00h |
| 0002E8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 0002E9h | UART1 Bit Rate Register | U1BRG | XXh |
| 0002EAh 0002EBh | UART1 Transmit Buffer Register | U1TB | XXXXh |
| 0002ECh | UART1 Transmit/Receive Control Register 0 | U1C0 | 0000 1000b |
| 0002EDh | UART1 Transmit/Receive Control Register 1 | U1C1 | 0000 0010b |
| 0002EEh 0002EFh | UART1 Receive Buffer Register | U1RB | XXXXh |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.12 SFR List (12)

| Address | Register | Symbol | Reset Value |
|---------|---|--------|-------------|
| 0002F0h | | | |
| 0002F1h | | | |
| 0002F2h | | | |
| 0002F3h | | | |
| 0002F4h | UART4 Special Mode Register 4 | U4SMR4 | 00h |
| 0002F5h | UART4 Special Mode Register 3 | U4SMR3 | 00h |
| 0002F6h | UART4 Special Mode Register 2 | U4SMR2 | 00h |
| 0002F7h | UART4 Special Mode Register | U4SMR | 00h |
| 0002F8h | UART4 Transmit/Receive Mode Register | U4MR | 00h |
| 0002F9h | UART4 Bit Rate Register | U4BRG | XXh |
| 0002FAh | UART4 Transmit Buffer Register | U4TB | XXXXh |
| 0002FBh | | | |
| 0002FCh | UART4 Transmit/Receive Control Register 0 | U4C0 | 0000 1000b |
| 0002FDh | UART4 Transmit/Receive Control Register 1 | U4C1 | 0000 0010b |
| 0002FEh | UART4 Receive Buffer Register | U4RB | XXXXh |
| 0002FFh | | | |
| 000300h | Count Start Register for Timers B3, B4, and B5 | TBSR | 000X XXXXb |
| 000301h | | | |
| 000302h | Timer A1-1 Register | TA11 | XXXXh |
| 000303h | | | |
| 000304h | Timer A2-1 Register | TA21 | XXXXh |
| 000305h | | | |
| 000306h | Timer A4-1 Register | TA41 | XXXXh |
| 000307h | | | |
| 000308h | Three-phase PWM Control Register 0 | INVC0 | 00h |
| 000309h | Three-phase PWM Control Register 1 | INVC1 | 00h |
| 00030Ah | Three-phase Output Buffer Register 0 | IDB0 | XX11 1111b |
| 00030Bh | Three-phase Output Buffer Register 1 | IDB1 | XX11 1111b |
| 00030Ch | Dead Time Timer | DTT | XXh |
| 00030Dh | Timer B2 Interrupt Generating Frequency Set Counter | ICTB2 | XXh |
| 00030Eh | | | |
| 00030Fh | | | |
| 000310h | Timer B3 Register | TB3 | XXXXh |
| 000311h | | | |
| 000312h | Timer B4 Register | TB4 | XXXXh |
| 000313h | | | |
| 000314h | Timer B5 Register | TB5 | XXXXh |
| 000315h | | | |
| 000316h | | | |
| 000317h | | | |
| 000318h | | | |
| 000319h | | | |
| 00031Ah | | | |
| 00031Bh | Timer B3 Mode Register | TB3MR | 00XX 0000b |
| 00031Ch | Timer B4 Mode Register | TB4MR | 00XX 0000b |
| 00031Dh | Timer B5 Mode Register | TB5MR | 00XX 0000b |
| 00031Eh | | | |
| 00031Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.13 SFR List (13)

| Address | Register | Symbol | Reset Value |
|---------|--|--------|-------------|
| 000320h | | | |
| 000321h | | | |
| 000322h | | | |
| 000323h | | | |
| 000324h | UART3 Special Mode Register 4 | U3SMR4 | 00h |
| 000325h | UART3 Special Mode Register 3 | U3SMR3 | 00h |
| 000326h | UART3 Special Mode Register 2 | U3SMR2 | 00h |
| 000327h | UART3 Special Mode Register | U3SMR | 00h |
| 000328h | UART3 Transmit/Receive Mode Register | U3MR | 00h |
| 000329h | UART3 Bit Rate Register | U3BRG | XXh |
| 00032Ah | UART3 Transmit Buffer Register | U3TB | XXXXh |
| 00032Bh | | | |
| 00032Ch | UART3 Transmit/Receive Control Register 0 | U3C0 | 0000 1000b |
| 00032Dh | UART3 Transmit/Receive Control Register 1 | U3C1 | 0000 0010b |
| 00032Eh | UART3 Receive Buffer Register | U3RB | XXXXh |
| 00032Fh | | | |
| 000330h | | | |
| 000331h | | | |
| 000332h | | | |
| 000333h | | | |
| 000334h | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 000335h | UART2 Special Mode Register 3 | U2SMR3 | 00h |
| 000336h | UART2 Special Mode Register 2 | U2SMR2 | 00h |
| 000337h | UART2 Special Mode Register | U2SMR | 00h |
| 000338h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 000339h | UART2 Bit Rate Register | U2BRG | XXh |
| 00033Ah | UART2 Transmit Buffer Register | U2TB | XXXXh |
| 00033Bh | | | |
| 00033Ch | UART2 Transmit/Receive Control Register 0 | U2C0 | 0000 1000b |
| 00033Dh | UART2 Transmit/Receive Control Register 1 | U2C1 | 0000 0010b |
| 00033Eh | UART2 Receive Buffer Register | U2RB | XXXXh |
| 00033Fh | | | |
| 000340h | Count Start Register | TABSR | 0000 0000b |
| 000341h | Clock Prescaler Reset Register | CPSRF | 0XXX XXXXb |
| 000342h | One-shot Start Register | ONSF | 0000 0000b |
| 000343h | Trigger Select Register | TRGSR | 0000 0000b |
| 000344h | Increment/Decrement Counting Select Register | UDF | 0000 0000b |
| 000345h | | | |
| 000346h | Timer A0 Register | TA0 | XXXXh |
| 000347h | | | |
| 000348h | Timer A1 Register | TA1 | XXXXh |
| 000349h | | | |
| 00034Ah | Timer A2 Register | TA2 | XXXXh |
| 00034Bh | | | |
| 00034Ch | Timer A3 Register | TA3 | XXXXh |
| 00034Dh | | | |
| 00034Eh | Timer A4 Register | TA4 | XXXXh |
| 00034Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.14 SFR List (14)

| Address | Register | Symbol | Reset Value |
|---------|---|--------|-------------|
| 000350h | Timer B0 Register | TB0 | XXXXh |
| 000351h | | | |
| 000352h | Timer B1 Register | TB1 | XXXXh |
| 000353h | | | |
| 000354h | Timer B2 Register | TB2 | XXXXh |
| 000355h | | | |
| 000356h | Timer A0 Mode Register | TA0MR | 0000 0000b |
| 000357h | Timer A1 Mode Register | TA1MR | 0000 0000b |
| 000358h | Timer A2 Mode Register | TA2MR | 0000 0000b |
| 000359h | Timer A3 Mode Register | TA3MR | 0000 0000b |
| 00035Ah | Timer A4 Mode Register | TA4MR | 0000 0000b |
| 00035Bh | Timer B0 Mode Register | TB0MR | 00XX 0000b |
| 00035Ch | Timer B1 Mode Register | TB1MR | 00XX 0000b |
| 00035Dh | Timer B2 Mode Register | TB2MR | 00XX 0000b |
| 00035Eh | Timer B2 Special Mode Register | TB2SC | XXXX XXX0b |
| 00035Fh | Count Source Prescaler Register | TCSPR | 0000 0000b |
| 000360h | | | |
| 000361h | | | |
| 000362h | | | |
| 000363h | | | |
| 000364h | UART0 Special Mode Register 4 | U0SMR4 | 00h |
| 000365h | UART0 Special Mode Register 3 | U0SMR3 | 00h |
| 000366h | UART0 Special Mode Register 2 | U0SMR2 | 00h |
| 000367h | UART0 Special Mode Register | U0SMR | 00h |
| 000368h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 000369h | UART0 Bit Rate Register | U0BRG | XXh |
| 00036Ah | UART0 Transmit Buffer Register | U0TB | XXXXh |
| 00036Bh | | | |
| 00036Ch | UART0 Transmit/Receive Control Register 0 | U0C0 | 0000 1000b |
| 00036Dh | UART0 Transmit/Receive Control Register 1 | U0C1 | 0000 0010b |
| 00036Eh | UART0 Receive Buffer Register | U0RB | XXXXh |
| 00036Fh | | | |
| 000370h | | | |
| 000371h | | | |
| 000372h | | | |
| 000373h | | | |
| 000374h | | | |
| 000375h | | | |
| 000376h | | | |
| 000377h | | | |
| 000378h | | | |
| 000379h | | | |
| 00037Ah | | | |
| 00037Bh | | | |
| 00037Ch | CRC Data Register | CRCD | XXXXh |
| 00037Dh | | | |
| 00037Eh | CRC Input Register | CRCIN | XXh |
| 00037Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------|---------|-------------|
| 000380h | A/D0 Register 0 | AD00 | 00XXh |
| 000381h | | | |
| 000382h | A/D0 Register 1 | AD01 | 00XXh |
| 000383h | | | |
| 000384h | A/D0 Register 2 | AD02 | 00XXh |
| 000385h | | | |
| 000386h | A/D0 Register 3 | AD03 | 00XXh |
| 000387h | | | |
| 000388h | A/D0 Register 4 | AD04 | 00XXh |
| 000389h | | | |
| 00038Ah | A/D0 Register 5 | AD05 | 00XXh |
| 00038Bh | | | |
| 00038Ch | A/D0 Register 6 | AD06 | 00XXh |
| 00038Dh | | | |
| 00038Eh | A/D0 Register 7 | AD07 | 00XXh |
| 00038Fh | | | |
| 000390h | | | |
| 000391h | | | |
| 000392h | A/D0 Control Register 4 | AD0CON4 | XXXX 00XXb |
| 000393h | A/D0 Control Register 5 | AD0CON5 | 00h |
| 000394h | A/D0 Control Register 2 | AD0CON2 | XX0X X000b |
| 000395h | A/D0 Control Register 3 | AD0CON3 | XXXX X000b |
| 000396h | A/D0 Control Register 0 | AD0CON0 | 00h |
| 000397h | A/D0 Control Register 1 | AD0CON1 | 00h |
| 000398h | D/A Register 0 | DA0 | XXh |
| 000399h | | | |
| 00039Ah | D/A Register 1 | DA1 | XXh |
| 00039Bh | | | |
| 00039Ch | D/A Control Register | DACON | XXXX XX00b |
| 00039Dh | | | |
| 00039Eh | | | |
| 00039Fh | | | |
| 0003A0h | | | |
| 0003A1h | | | |
| 0003A2h | | | |
| 0003A3h | | | |
| 0003A4h | | | |
| 0003A5h | | | |
| 0003A6h | | | |
| 0003A7h | | | |
| 0003A8h | | | |
| 0003A9h | | | |
| 0003AAh | | | |
| 0003ABh | | | |
| 0003ACh | | | |
| 0003ADh | | | |
| 0003AEh | | | |
| 0003AFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.16 SFR List (16)

| Address | Register | Symbol | Reset Value |
|---------|-----------------------------|--------|-------------|
| 0003B0h | | | |
| 0003B1h | | | |
| 0003B2h | | | |
| 0003B3h | | | |
| 0003B4h | | | |
| 0003B5h | | | |
| 0003B6h | | | |
| 0003B7h | | | |
| 0003B8h | | | |
| 0003B9h | | | |
| 0003BAh | | | |
| 0003BBh | | | |
| 0003BCh | | | |
| 0003BDh | | | |
| 0003BEh | | | |
| 0003BFh | | | |
| 0003C0h | Port P0 Register | P0 | XXh |
| 0003C1h | Port P1 Register | P1 | XXh |
| 0003C2h | Port P0 Direction Register | PD0 | 0000 0000b |
| 0003C3h | Port P1 Direction Register | PD1 | 0000 0000b |
| 0003C4h | Port P2 Register | P2 | XXh |
| 0003C5h | Port P3 Register | P3 | XXh |
| 0003C6h | Port P2 Direction Register | PD2 | 0000 0000b |
| 0003C7h | Port P3 Direction Register | PD3 | 0000 0000b |
| 0003C8h | Port P4 Register | P4 | XXh |
| 0003C9h | Port P5 Register | P5 | XXh |
| 0003CAh | Port P4 Direction Register | PD4 | 0000 0000b |
| 0003CBh | Port P5 Direction Register | PD5 | 0000 0000b |
| 0003CCh | Port P6 Register | P6 | XXh |
| 0003CDh | Port P7 Register | P7 | XXh |
| 0003CEh | Port P6 Direction Register | PD6 | 0000 0000b |
| 0003CFh | Port P7 Direction Register | PD7 | 0000 0000b |
| 0003D0h | Port P8 Register | P8 | XXh |
| 0003D1h | Port P9 Register | P9 | XXh |
| 0003D2h | Port P8 Direction Register | PD8 | 00X0 0000b |
| 0003D3h | Port P9 Direction Register | PD9 | 0000 0000b |
| 0003D4h | Port P10 Register | P10 | XXh |
| 0003D5h | Port P11 Register | P11 | XXh |
| 0003D6h | Port P10 Direction Register | PD10 | 0000 0000b |
| 0003D7h | Port P11 Direction Register | PD11 | 0000 0000b |
| 0003D8h | Port P12 Register | P12 | XXh |
| 0003D9h | Port P13 Register | P13 | XXh |
| 0003DAh | Port P12 Direction Register | PD12 | 0000 0000b |
| 0003DBh | Port P13 Direction Register | PD13 | 0000 0000b |
| 0003DCh | Port P14 Register | P14 | XXh |
| 0003DDh | Port P15 Register | P15 | XXh |
| 0003DEh | Port P14 Direction Register | PD14 | 0000 0000b |
| 0003DFh | Port P15 Direction Register | PD15 | 0000 0000b |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

| Address | Register | Symbol | Reset Value |
|---------|-----------------------------|--------|----------------|
| 0003E0h | Port P16 Register | P16 | XXh |
| 0003E1h | Port P17 Register | P17 | XXh |
| 0003E2h | Port P16 Direction Register | PD16 | 0000 0000b |
| 0003E3h | Port P17 Direction Register | PD17 | 0000 0000b |
| 0003E4h | Port P18 Register | P18 | XXh |
| 0003E5h | Port P19 Register | P19 | XXh |
| 0003E6h | Port P18 Direction Register | PD18 | 0000 0000b |
| 0003E7h | Port P19 Direction Register | PD19 | 0000 0000b |
| 0003E8h | | | |
| 0003E9h | | | |
| 0003EAh | | | |
| 0003EBh | | | |
| 0003ECh | | | |
| 0003EDh | | | |
| 0003EEh | | | |
| 0003EFh | | | |
| 0003F0h | Pull-up Control Register 0 | PUR0 | 0000 0000b |
| 0003F1h | Pull-up Control Register 1 | PUR1 | XXXX X0XXb |
| 0003F2h | Pull-up Control Register 2 | PUR2 | X00X XXXXb |
| 0003F3h | Pull-up Control Register 3 | PUR3 | 00XX 0000b |
| 0003F4h | Pull-up Control Register 4 | PUR4 | 0XXX 0000b |
| 0003F5h | Pull-up Control Register 5 | PUR5 | XXXX 0000b |
| 0003F6h | | | |
| 0003F7h | | | |
| 0003F8h | | | |
| 0003F9h | | | |
| 0003FAh | | | |
| 0003FBh | | | |
| 0003FCh | | | |
| 0003FDh | | | |
| 0003FEh | | | |
| 0003FFh | Port Control Register | PCR | ?0XX 0XX0b (1) |

X: Undefined

Blanks are reserved. No access is allowed.

Note:

1. The bit 7 is 0 in the 144-pin package and 1 in the 176-pin package.

Table 4.18 SFR List (18)

| Address | Register | Symbol | Reset Value |
|---------|---|--------|---------------|
| 040000h | Flash Memory Control Register 0 | FMR0 | 0001 XX00b |
| 040001h | Flash Memory Status Register 0 | FMSR0 | 1000 0000b |
| 040002h | | | |
| 040003h | | | |
| 040004h | | | |
| 040005h | | | |
| 040006h | | | |
| 040007h | | | |
| 040008h | Flash Register Protection Unlock Register 0 | FPR0 | 00h |
| 040009h | Flash Memory Control Register 1 | FMR1 | 0000 0010b |
| 04000Ah | Block Protect Bit Monitor Register 0 | FBPM0 | ??X? ???b (1) |
| 04000Bh | Block Protect Bit Monitor Register 1 | FBPM1 | XXX? ???b (1) |
| 04000Ch | | | |
| 04000Dh | | | |
| 04000Eh | | | |
| 04000Fh | | | |
| 040010h | | | |
| 040011h | Block Protect Bit Monitor Register 2 | FBPM2 | ???? ???b (1) |
| 040012h | | | |
| 040013h | | | |
| 040014h | | | |
| 040015h | | | |
| 040016h | | | |
| 040017h | | | |
| 040018h | | | |
| 040019h | | | |
| 04001Ah | | | |
| 04001Bh | | | |
| 04001Ch | | | |
| 04001Dh | | | |
| 04001Eh | | | |
| 04001Fh | | | |
| 040020h | PLL Control Register 0 | PLC0 | 0000 0001b |
| 040021h | PLL Control Register 1 | PLC1 | 0001 1111b |
| 040022h | | | |
| 040023h | | | |
| 040024h | | | |
| 040025h | | | |
| 040026h | | | |
| 040027h | | | |
| 040028h | | | |
| 040029h | | | |
| 04002Ah | | | |
| 04002Bh | | | |
| 04002Ch | | | |
| 04002Dh | | | |
| 04002Eh | | | |
| 04002Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Note:

1. The status of protect bit of each block in flash memory is reflected.

Table 4.19 SFR List (19)

| Address | Register | Symbol | Reset Value |
|-----------------------|---|--------|---|
| 040030h to 04003Fh | | | |
| 040040h | | | |
| 040041h | | | |
| 040042h | | | |
| 040043h | | | |
| 040044h | Processor Mode Register 0 ⁽¹⁾ | PM0 | 1000 0000b (CNVSS pin = Low) 0000 0011b (CNVSS pin = High) |
| 040045h | | | |
| 040046h | System Clock Control Register 0 | CM0 | 0000 1000b |
| 040047h | System Clock Control Register 1 | CM1 | 0010 0000b |
| 040048h | Processor Mode Register 3 | PM3 | 00h |
| 040049h | | | |
| 04004Ah | Protect Register | PRCR | XXXX X000b |
| 04004Bh | | | |
| 04004Ch | Protect Register 3 | PRCR3 | 0000 0000b |
| 04004Dh | Oscillator Stop Detection Register | CM2 | 00h |
| 04004Eh | | | |
| 04004Fh | | | |
| 040050h | | | |
| 040051h | | | |
| 040052h | | | |
| 040053h | Processor Mode Register 2 | PM2 | 00h |
| 040054h | Chip Select Output Pin Setting Register 0 | CSOP0 | 1000 XXXXb |
| 040055h | Chip Select Output Pin Setting Register 1 | CSOP1 | 01X0 XXXXb |
| 040056h | Chip Select Output Pin Setting Register 2 | CSOP2 | XXXX 0000b |
| 040057h | | | |
| 040058h | | | |
| 040059h | | | |
| 04005Ah | Low Speed Mode Clock Control Register | CM3 | XXXX XX00b |
| 04005Bh | | | |
| 04005Ch | | | |
| 04005Dh | | | |
| 04005Eh | | | |
| 04005Fh | | | |
| 040060h | Voltage Regulator Control Register | VRCR | 0000 0000b |
| 040061h | | | |
| 040062h | Low Voltage Detector Control Register | LVDC | 0000 XX00b |
| 040063h | | | |
| 040064h | Detection Voltage Configuration Register | DVCR | 0000 XXXXb |
| 040065h | | | |
| 040066h | | | |
| 040067h | | | |
| 040068h to 040093h | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Note:

1. The value in the PM0 register remains unchanged even after a software reset or watchdog timer reset.

Table 4.20 SFR List (20)

| Address | Register | Symbol | Reset Value |
|---------|--|--------|-------------|
| 040094h | | | |
| 040095h | | | |
| 040096h | | | |
| 040097h | Three-phase Output Buffer Control Register | IOBC | 0XXX XXXXb |
| 040098h | Input Function Select Register 0 | IFS0 | X000 0000b |
| 040099h | Input Function Select Register 1 | IFS1 | XXXX X0X0b |
| 04009Ah | Input Function Select Register 2 | IFS2 | 0000 00X0b |
| 04009Bh | Input Function Select Register 3 | IFS3 | XX00 XX00b |
| 04009Ch | | | |
| 04009Dh | | | |
| 04009Eh | | | |
| 04009Fh | | | |
| 0400A0h | Port P0_0 Function Select Register | P0_0S | 0XXX X000b |
| 0400A1h | Port P1_0 Function Select Register | P1_0S | XXXX X000b |
| 0400A2h | Port P0_1 Function Select Register | P0_1S | 0XXX X000b |
| 0400A3h | Port P1_1 Function Select Register | P1_1S | XXXX X000b |
| 0400A4h | Port P0_2 Function Select Register | P0_2S | 0XXX X000b |
| 0400A5h | Port P1_2 Function Select Register | P1_2S | XXXX X000b |
| 0400A6h | Port P0_3 Function Select Register | P0_3S | 0XXX X000b |
| 0400A7h | Port P1_3 Function Select Register | P1_3S | XXXX X000b |
| 0400A8h | Port P0_4 Function Select Register | P0_4S | 0XXX X000b |
| 0400A9h | Port P1_4 Function Select Register | P1_4S | XXXX X000b |
| 0400AAh | Port P0_5 Function Select Register | P0_5S | 0XXX X000b |
| 0400ABh | Port P1_5 Function Select Register | P1_5S | XXXX X000b |
| 0400ACh | Port P0_6 Function Select Register | P0_6S | 0XXX X000b |
| 0400ADh | Port P1_6 Function Select Register | P1_6S | XXXX X000b |
| 0400AEh | Port P0_7 Function Select Register | P0_7S | 0XXX X000b |
| 0400AFh | Port P1_7 Function Select Register | P1_7S | XXXX X000b |
| 0400B0h | Port P2_0 Function Select Register | P2_0S | 00XX X000b |
| 0400B1h | Port P3_0 Function Select Register | P3_0S | XXXX X000b |
| 0400B2h | Port P2_1 Function Select Register | P2_1S | 00XX X000b |
| 0400B3h | Port P3_1 Function Select Register | P3_1S | XXXX X000b |
| 0400B4h | Port P2_2 Function Select Register | P2_2S | 00XX X000b |
| 0400B5h | Port P3_2 Function Select Register | P3_2S | XXXX X000b |
| 0400B6h | Port P2_3 Function Select Register | P2_3S | 00XX X000b |
| 0400B7h | Port P3_3 Function Select Register | P3_3S | XXXX X000b |
| 0400B8h | Port P2_4 Function Select Register | P2_4S | 00XX X000b |
| 0400B9h | Port P3_4 Function Select Register | P3_4S | XXXX X000b |
| 0400BAh | Port P2_5 Function Select Register | P2_5S | 00XX X000b |
| 0400BBh | Port P3_5 Function Select Register | P3_5S | XXXX X000b |
| 0400BCh | Port P2_6 Function Select Register | P2_6S | 00XX X000b |
| 0400BDh | Port P3_6 Function Select Register | P3_6S | XXXX X000b |
| 0400BEh | Port P2_7 Function Select Register | P2_7S | 00XX X000b |
| 0400BFh | Port P3_7 Function Select Register | P3_7S | XXXX X000b |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.21 SFR List (21)

| Address | Register | Symbol | Reset Value |
|---------|------------------------------------|--------|-------------|
| 0400C0h | Port P4_0 Function Select Register | P4_0S | X0XX X000b |
| 0400C1h | Port P5_0 Function Select Register | P5_0S | XXXX X000b |
| 0400C2h | Port P4_1 Function Select Register | P4_1S | X0XX X000b |
| 0400C3h | Port P5_1 Function Select Register | P5_1S | XXXX X000b |
| 0400C4h | Port P4_2 Function Select Register | P4_2S | X0XX X000b |
| 0400C5h | Port P5_2 Function Select Register | P5_2S | XXXX X000b |
| 0400C6h | Port P4_3 Function Select Register | P4_3S | X0XX X000b |
| 0400C7h | Port P5_3 Function Select Register | P5_3S | XXXX X000b |
| 0400C8h | Port P4_4 Function Select Register | P4_4S | X0XX X000b |
| 0400C9h | Port P5_4 Function Select Register | P5_4S | X0XX X000b |
| 0400CAh | Port P4_5 Function Select Register | P4_5S | X0XX X000b |
| 0400CBh | Port P5_5 Function Select Register | P5_5S | X0XX X000b |
| 0400CCh | Port P4_6 Function Select Register | P4_6S | X0XX X000b |
| 0400CDh | Port P5_6 Function Select Register | P5_6S | X0XX X000b |
| 0400CEh | Port P4_7 Function Select Register | P4_7S | X0XX X000b |
| 0400CFh | Port P5_7 Function Select Register | P5_7S | X0XX X000b |
| 0400D0h | Port P6_0 Function Select Register | P6_0S | X0XX X000b |
| 0400D1h | Port P7_0 Function Select Register | P7_0S | X0XX X000b |
| 0400D2h | Port P6_1 Function Select Register | P6_1S | X0XX X000b |
| 0400D3h | Port P7_1 Function Select Register | P7_1S | X0XX X000b |
| 0400D4h | Port P6_2 Function Select Register | P6_2S | X0XX X000b |
| 0400D5h | Port P7_2 Function Select Register | P7_2S | X0XX X000b |
| 0400D6h | Port P6_3 Function Select Register | P6_3S | X0XX X000b |
| 0400D7h | Port P7_3 Function Select Register | P7_3S | X0XX X000b |
| 0400D8h | Port P6_4 Function Select Register | P6_4S | X0XX X000b |
| 0400D9h | Port P7_4 Function Select Register | P7_4S | X0XX X000b |
| 0400DAh | Port P6_5 Function Select Register | P6_5S | X0XX X000b |
| 0400DBh | Port P7_5 Function Select Register | P7_5S | X0XX X000b |
| 0400DCh | Port P6_6 Function Select Register | P6_6S | X0XX X000b |
| 0400DDh | Port P7_6 Function Select Register | P7_6S | X0XX X000b |
| 0400DEh | Port P6_7 Function Select Register | P6_7S | X0XX X000b |
| 0400DFh | Port P7_7 Function Select Register | P7_7S | X0XX X000b |
| 0400E0h | Port P8_0 Function Select Register | P8_0S | X0XX X000b |
| 0400E1h | Port P9_0 Function Select Register | P9_0S | X0XX X000b |
| 0400E2h | Port P8_1 Function Select Register | P8_1S | X0XX X000b |
| 0400E3h | Port P9_1 Function Select Register | P9_1S | X0XX X000b |
| 0400E4h | Port P8_2 Function Select Register | P8_2S | X0XX X000b |
| 0400E5h | Port P9_2 Function Select Register | P9_2S | X0XX X000b |
| 0400E6h | Port P8_3 Function Select Register | P8_3S | X0XX X000b |
| 0400E7h | Port P9_3 Function Select Register | P9_3S | 00XX X000b |
| 0400E8h | Port P8_4 Function Select Register | P8_4S | XXXX X000b |
| 0400E9h | Port P9_4 Function Select Register | P9_4S | 00XX X000b |
| 0400EAh | | | |
| 0400EBh | Port P9_5 Function Select Register | P9_5S | 00XX X000b |
| 0400ECh | Port P8_6 Function Select Register | P8_6S | XXXX X000b |
| 0400EDh | Port P9_6 Function Select Register | P9_6S | 00XX X000b |
| 0400EEh | Port P8_7 Function Select Register | P8_7S | XXXX X000b |
| 0400EFh | Port P9_7 Function Select Register | P9_7S | X0XX X000b |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.22 SFR List (22)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------|
| 0400F0h | Port P10_0 Function Select Register | P10_0S | 0XXX X000b |
| 0400F1h | Port P11_0 Function Select Register | P11_0S | X0XX X000b |
| 0400F2h | Port P10_1 Function Select Register | P10_1S | 0XXX X000b |
| 0400F3h | Port P11_1 Function Select Register | P11_1S | X0XX X000b |
| 0400F4h | Port P10_2 Function Select Register | P10_2S | 0XXX X000b |
| 0400F5h | Port P11_2 Function Select Register | P11_2S | X0XX X000b |
| 0400F6h | Port P10_3 Function Select Register | P10_3S | 0XXX X000b |
| 0400F7h | Port P11_3 Function Select Register | P11_3S | X0XX X000b |
| 0400F8h | Port P10_4 Function Select Register | P10_4S | 0XXX X000b |
| 0400F9h | Port P11_4 Function Select Register | P11_4S | XXXX X000b |
| 0400FAh | Port P10_5 Function Select Register | P10_5S | 0XXX X000b |
| 0400FBh | Port P11_5 Function Select Register | P11_5S | XXXX X000b |
| 0400FCh | Port P10_6 Function Select Register | P10_6S | 0XXX X000b |
| 0400FDh | Port P11_6 Function Select Register | P11_6S | XXXX X000b |
| 0400FEh | Port P10_7 Function Select Register | P10_7S | 0XXX X000b |
| 0400FFh | Port P11_7 Function Select Register | P11_7S | XXXX X000b |
| 040100h | Port P12_0 Function Select Register | P12_0S | X0XX X000b |
| 040101h | Port P13_0 Function Select Register | P13_0S | XXXX X000b |
| 040102h | Port P12_1 Function Select Register | P12_1S | X0XX X000b |
| 040103h | Port P13_1 Function Select Register | P13_1S | XXXX X000b |
| 040104h | Port P12_2 Function Select Register | P12_2S | X0XX X000b |
| 040105h | Port P13_2 Function Select Register | P13_2S | XXXX X000b |
| 040106h | Port P12_3 Function Select Register | P12_3S | X0XX X000b |
| 040107h | Port P13_3 Function Select Register | P13_3S | XXXX X000b |
| 040108h | Port P12_4 Function Select Register | P12_4S | X0XX X000b |
| 040109h | Port P13_4 Function Select Register | P13_4S | XXXX X000b |
| 04010Ah | Port P12_5 Function Select Register | P12_5S | X0XX X000b |
| 04010Bh | Port P13_5 Function Select Register | P13_5S | XXXX X000b |
| 04010Ch | Port P12_6 Function Select Register | P12_6S | X0XX X000b |
| 04010Dh | Port P13_6 Function Select Register | P13_6S | XXXX X000b |
| 04010Eh | Port P12_7 Function Select Register | P12_7S | X0XX X000b |
| 04010Fh | Port P13_7 Function Select Register | P13_7S | XXXX X000b |
| 040110h | | | |
| 040111h | Port P15_0 Function Select Register | P15_0S | 00XX X000b |
| 040112h | | | |
| 040113h | Port P15_1 Function Select Register | P15_1S | 00XX X000b |
| 040114h | | | |
| 040115h | Port P15_2 Function Select Register | P15_2S | 00XX X000b |
| 040116h | Port P14_3 Function Select Register | P14_3S | XXXX X000b |
| 040117h | Port P15_3 Function Select Register | P15_3S | 00XX X000b |
| 040118h | Port P14_4 Function Select Register | P14_4S | XXXX X000b |
| 040119h | Port P15_4 Function Select Register | P15_4S | 00XX X000b |
| 04011Ah | Port P14_5 Function Select Register | P14_5S | XXXX X000b |
| 04011Bh | Port P15_5 Function Select Register | P15_5S | 00XX X000b |
| 04011Ch | Port P14_6 Function Select Register | P14_6S | XXXX X000b |
| 04011Dh | Port P15_6 Function Select Register | P15_6S | 00XX X000b |
| 04011Eh | Port P14_7 Function Select Register | P14_7S | XXXX X000b |
| 04011Fh | Port P15_7 Function Select Register | P15_7S | 00XX X000b |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.23 SFR List (23)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------|
| 040120h | Port P16_0 Function Select Register | P16_0S | X0XX X000b |
| 040121h | Port P17_0 Function Select Register | P17_0S | X0XX X000b |
| 040122h | Port P16_1 Function Select Register | P16_1S | X0XX X000b |
| 040123h | Port P17_1 Function Select Register | P17_1S | X0XX X000b |
| 040124h | Port P16_2 Function Select Register | P16_2S | X0XX X000b |
| 040125h | Port P17_2 Function Select Register | P17_2S | X0XX X000b |
| 040126h | Port P16_3 Function Select Register | P16_3S | X0XX X000b |
| 040127h | Port P17_3 Function Select Register | P17_3S | X0XX X000b |
| 040128h | Port P16_4 Function Select Register | P16_4S | X0XX X000b |
| 040129h | Port P17_4 Function Select Register | P17_4S | XXXX X000b |
| 04012Ah | Port P16_5 Function Select Register | P16_5S | X0XX X000b |
| 04012Bh | Port P17_5 Function Select Register | P17_5S | XXXX X000b |
| 04012Ch | Port P16_6 Function Select Register | P16_6S | X0XX X000b |
| 04012Dh | Port P17_6 Function Select Register | P17_6S | XXXX X000b |
| 04012Eh | Port P16_7 Function Select Register | P16_7S | X0XX X000b |
| 04012Fh | Port P17_7 Function Select Register | P17_7S | XXXX X000b |
| 040130h | Port P18_0 Function Select Register | P18_0S | XXXX X000b |
| 040131h | Port P19_0 Function Select Register | P19_0S | XXXX X000b |
| 040132h | Port P18_1 Function Select Register | P18_1S | XXXX X000b |
| 040133h | Port P19_1 Function Select Register | P19_1S | XXXX X000b |
| 040134h | Port P18_2 Function Select Register | P18_2S | XXXX X000b |
| 040135h | Port P19_2 Function Select Register | P19_2S | XXXX X000b |
| 040136h | Port P18_3 Function Select Register | P18_3S | XXXX X000b |
| 040137h | Port P19_3 Function Select Register | P19_3S | XXXX X000b |
| 040138h | Port P18_4 Function Select Register | P18_4S | XXXX X000b |
| 040139h | Port P19_4 Function Select Register | P19_4S | XXXX X000b |
| 04013Ah | Port P18_5 Function Select Register | P18_5S | XXXX X000b |
| 04013Bh | Port P19_5 Function Select Register | P19_5S | XXXX X000b |
| 04013Ch | Port P18_6 Function Select Register | P18_6S | XXXX X000b |
| 04013Dh | Port P19_6 Function Select Register | P19_6S | XXXX X000b |
| 04013Eh | Port P18_7 Function Select Register | P18_7S | XXXX X000b |
| 04013Fh | Port P19_7 Function Select Register | P19_7S | XXXX X000b |
| 040140h | | | |
| 040141h | | | |
| 040142h | | | |
| 040143h | | | |
| 040144h | | | |
| 040145h | | | |
| 040146h | | | |
| 040147h | | | |
| 040148h | | | |
| 040149h | | | |
| 04014Ah | | | |
| 04014Bh | | | |
| 04014Ch | | | |
| 04014Dh | | | |
| 04014Eh | | | |
| 04014Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.24 SFR List (24)

| Address | Register | Symbol | Reset Value |
|-----------------------|---|---------|-------------|
| 040150h to 0402FFh | | | |
| 040300h | UART9 Transmit/Receive Mode Register | U9MR | 00h |
| 040301h | UART9 Bit Rate Register | U9BRG | XXh |
| 040302h | UART9 Transmit Buffer Register | U9TB | XXXXh |
| 040303h | | | |
| 040304h | UART9 Transmit/Receive Control Register 0 | U9C0 | 00X0 1000b |
| 040305h | UART9 Transmit/Receive Control Register 1 | U9C1 | XXXX 0010b |
| 040306h | UART9 Receive Buffer Register | U9RB | XXXXh |
| 040307h | | | |
| 040308h | UART10 Transmit/Receive Mode Register | U10MR | 00h |
| 040309h | UART10 Bit Rate Register | U10BRG | XXh |
| 04030Ah | UART10 Transmit Buffer Register | U10TB | XXXXh |
| 04030Bh | | | |
| 04030Ch | UART10 Transmit/Receive Control Register 0 | U10C0 | 00X0 1000b |
| 04030Dh | UART10 Transmit/Receive Control Register 1 | U10C1 | XXXX 0010b |
| 04030Eh | UART10 Receive Buffer Register | U10RB | XXXXh |
| 04030Fh | | | |
| 040310h | UART9, UART10 Transmit/Receive Control Register 2 | U910CON | X000 0000b |
| 040311h | | | |
| 040312h | | | |
| 040313h | | | |
| 040314h | | | |
| 040315h | | | |
| 040316h | | | |
| 040317h | | | |
| 040318h to 041FFFh | | | |
| 042000h to 04201Fh | Protected Area 0 | — | Undefined |
| 042020h to 04203Fh | Protected Area 1 | — | Undefined |
| 042040h to 04205Fh | Protected Area 2 | — | Undefined |
| 042060h to 04207Fh | Protected Area 3 | — | Undefined |
| 042080h to 04209Fh | Protected Area 4 | — | Undefined |
| 0420A0h to 0420EFh | | | |
| 0420F0h | Protected Area Protect Release Register | PAPR | XXX0 0000b |
| 0420F1h | | | |
| 0420F2h | Protected Area Write Access Flag Register | PAWF | XXX0 0000b |
| 0420F3h | | | |
| 0420F4h | | | |
| 0420F5h | | | |
| 0420F6h | | | |
| 0420F7h | | | |
| 0420F8h to 043FFFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.25 SFR List (25)

| Address | Register | Symbol | Reset Value |
|-----------------------|---------------------------------------|--------|---------------------------|
| 044000h to 04403Fh | | | |
| 044040h | | | |
| 044041h | | | |
| 044042h | | | |
| 044043h | | | |
| 044044h | | | |
| 044045h | | | |
| 044046h | | | |
| 044047h | | | |
| 044048h | | | |
| 044049h | | | |
| 04404Ah | | | |
| 04404Bh | | | |
| 04404Ch | Protect Register 4 | PRCR4 | 0000 0000b |
| 04404Dh | Watchdog Timer Clock Control Register | WDK | 0000 000?b ⁽¹⁾ |
| 04404Eh | Watchdog Timer Start Register | WDTS | XXXX XXXXb |
| 04404Fh | Watchdog Timer Control Register | WDC | 000X XXXXb |
| 044050h | | | |
| 044051h | | | |
| 044052h | | | |
| 044053h | | | |
| 044054h | | | |
| 044055h | | | |
| 044056h | | | |
| 044057h | | | |
| 044058h | | | |
| 044059h | | | |
| 04405Ah | | | |
| 04405Bh | | | |
| 04405Ch | | | |
| 04405Dh | | | |
| 04405Eh | | | |
| 04405Fh | Protect Register 2 | PRCR2 | 0XXX XXXXb |

X: Undefined

Blanks are reserved. No access is allowed.

Note:

1. The bit 0 is set to 1 when the most recent reset is caused by the watchdog timer. Otherwise, it is set to 0.

Table 4.26 SFR List (26)

| Address | Register | Symbol | Reset Value |
|---------|---|--------|-------------|
| 044060h | | | |
| 044061h | | | |
| 044062h | | | |
| 044063h | | | |
| 044064h | | | |
| 044065h | | | |
| 044066h | | | |
| 044067h | | | |
| 044068h | | | |
| 044069h | | | |
| 04406Ah | | | |
| 04406Bh | | | |
| 04406Ch | | | |
| 04406Dh | External Interrupt Request Source Select Register 1 | IFSR1 | X0XX X000b |
| 04406Eh | | | |
| 04406Fh | External Interrupt Request Source Select Register 0 | IFSR0 | 0000 0000b |
| 044070h | DMA0 Request Source Select Register 2 | DM0SL2 | XX00 0000b |
| 044071h | DMA1 Request Source Select Register 2 | DM1SL2 | XX00 0000b |
| 044072h | DMA2 Request Source Select Register 2 | DM2SL2 | XX00 0000b |
| 044073h | DMA3 Request Source Select Register 2 | DM3SL2 | XX00 0000b |
| 044074h | | | |
| 044075h | | | |
| 044076h | | | |
| 044077h | | | |
| 044078h | DMA0 Request Source Select Register | DM0SL | XXX0 0000b |
| 044079h | DMA1 Request Source Select Register | DM1SL | XXX0 0000b |
| 04407Ah | DMA2 Request Source Select Register | DM2SL | XXX0 0000b |
| 04407Bh | DMA3 Request Source Select Register | DM3SL | XXX0 0000b |
| 04407Ch | | | |
| 04407Dh | Wake-up IPL Setting Register 2 | RIPL2 | XX0X 0000b |
| 04407Eh | | | |
| 04407Fh | Wake-up IPL Setting Register 1 | RIPL1 | XX0X 0000b |
| 044080h | | | |
| 044081h | | | |
| 044082h | | | |
| 044083h | | | |
| 044084h | | | |
| 044085h | | | |
| 044086h | | | |
| 044087h | | | |
| 044088h | | | |
| 044089h | | | |
| 04408Ah | | | |
| 04408Bh | | | |
| 04408Ch | | | |
| 04408Dh | | | |
| 04408Eh | | | |
| 04408Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.27 SFR List (27)

| Address | Register | Symbol | Reset Value |
|-----------------------|--|---------|-------------|
| 044090h to 0443FFh | | | |
| 044400h | I ² C Bus Transmit/Receive Shift Register | I2CTRSR | XXh |
| 044401h | | | |
| 044402h | I ² C Bus Slave Address Register | I2CSAR | 00h |
| 044403h | I ² C Bus Control Register 0 | I2CCR0 | 0000 0000b |
| 044404h | I ² C Bus Clock Control Register | I2CCCR | 0000 0000b |
| 044405h | I ² C Bus START Condition/STOP Condition Control Register | I2CSSCR | 0000 0000b |
| 044406h | I ² C Bus Control Register 1 | I2CCR1 | 0000 0000b |
| 044407h | I ² C Bus Control Register 2 | I2CCR2 | 0000 0000b |
| 044408h | I ² C Bus Status Register | I2CSR | 0000 0000b |
| 044409h | | | |
| 04440Ah | | | |
| 04440Bh | | | |
| 04440Ch | | | |
| 04440Dh | | | |
| 04440Eh | | | |
| 04440Fh | | | |
| 044410h | I ² C Bus Mode Register | I2CMR | 0000 0000b |
| 044411h | | | |
| 044412h | | | |
| 044413h | | | |
| 044414h | | | |
| 044415h | | | |
| 044416h | | | |
| 044417h | | | |
| 044418h | | | |
| 044419h | | | |
| 04441Ah | | | |
| 04441Bh | | | |
| 04441Ch | | | |
| 04441Dh | | | |
| 04441Eh | | | |
| 04441Fh | | | |
| 044420h to 0467FFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.28 SFR List (28)

| Address | Register | Symbol | Reset Value | | | | |
|--|------------------------------------|--------|-------------|-------|------------|-------|------------|
| 046800h to 0477FFh | | | | | | | |
| 047800h 047801h 047802h 047803h 047804h | CAN1 Mailbox 0: Message Identifier | C1MB0 | XXXX XXXXh | | | | |
| 047805h | CAN1 Mailbox 0: Data Length | | | | | | |
| 047806h 047807h 047808h 047809h 04780Ah 04780Bh 04780Ch 04780Dh | CAN1 Mailbox 0: Data Field | | | | | | |
| 04780Eh 04780Fh | CAN1 Mailbox 0: Time Stamp | | | | | | |
| 047810h 047811h 047812h 047813h 047814h | CAN1 Mailbox 1: Message Identifier | | | C1MB1 | XXXX XXXXh | | |
| 047815h | CAN1 Mailbox 1: Data Length | | | | | | |
| 047816h 047817h 047818h 047819h 04781Ah 04781Bh 04781Ch 04781Dh | CAN1 Mailbox 1: Data Field | | | | | | |
| 04781Eh 04781Fh | CAN1 Mailbox 1: Time Stamp | | | | | | |
| 047820h 047821h 047822h 047823h 047824h | CAN1 Mailbox 2: Message Identifier | | | | | C1MB2 | XXXX XXXXh |
| 047825h | CAN1 Mailbox 2: Data Length | | | | | | |
| 047826h 047827h 047828h 047829h 04782Ah 04782Bh 04782Ch 04782Dh | CAN1 Mailbox 2: Data Field | | | | | | |
| 04782Eh 04782Fh | CAN1 Mailbox 2: Time Stamp | | | | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.29 SFR List (29)

| Address | Register | Symbol | Reset Value |
|---------|------------------------------------|--------|-------------------------|
| 047830h | CAN1 Mailbox 3: Message Identifier | C1MB3 | XXXX XXXXh |
| 047831h | | | |
| 047832h | | | |
| 047833h | | | |
| 047834h | | | |
| 047835h | CAN1 Mailbox 3: Data Length | | XXh |
| 047836h | CAN1 Mailbox 3: Data Field | | XXXX XXXX XXXX XXXXh |
| 047837h | | | |
| 047838h | | | |
| 047839h | | | |
| 04783Ah | | | |
| 04783Bh | | | |
| 04783Ch | | | |
| 04783Dh | | | |
| 04783Eh | CAN1 Mailbox 3: Time Stamp | | XXXXh |
| 04783Fh | | | |
| 047840h | CAN1 Mailbox 4: Message Identifier | C1MB4 | XXXX XXXXh |
| 047841h | | | |
| 047842h | | | |
| 047843h | | | |
| 047844h | | | |
| 047845h | CAN1 Mailbox 4: Data Length | | XXh |
| 047846h | CAN1 Mailbox 4: Data Field | | XXXX XXXX XXXX XXXXh |
| 047847h | | | |
| 047848h | | | |
| 047849h | | | |
| 04784Ah | | | |
| 04784Bh | | | |
| 04784Ch | | | |
| 04784Dh | | | |
| 04784Eh | CAN1 Mailbox 4: Time Stamp | | XXXXh |
| 04784Fh | | | |
| 047850h | CAN1 Mailbox 5: Message Identifier | C1MB5 | XXXX XXXXh |
| 047851h | | | |
| 047852h | | | |
| 047853h | | | |
| 047854h | | | |
| 047855h | CAN1 Mailbox 5: Data Length | | XXh |
| 047856h | CAN1 Mailbox 5: Data Field | | XXXX XXXX XXXX XXXXh |
| 047857h | | | |
| 047858h | | | |
| 047859h | | | |
| 04785Ah | | | |
| 04785Bh | | | |
| 04785Ch | | | |
| 04785Dh | | | |
| 04785Eh | CAN1 Mailbox 5: Time Stamp | | XXXXh |
| 04785Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.30 SFR List (30)

| Address | Register | Symbol | Reset Value |
|---------|------------------------------------|--------|-------------------------|
| 047860h | CAN1 Mailbox 6: Message Identifier | C1MB6 | XXXX XXXXh |
| 047861h | | | |
| 047862h | | | |
| 047863h | | | |
| 047864h | | | |
| 047865h | CAN1 Mailbox 6: Data Length | | XXh |
| 047866h | CAN1 Mailbox 6: Data Field | | XXXX XXXX XXXX XXXXh |
| 047867h | | | |
| 047868h | | | |
| 047869h | | | |
| 04786Ah | | | |
| 04786Bh | | | |
| 04786Ch | | | |
| 04786Dh | | | |
| 04786Eh | | | |
| 04786Fh | | | |
| 047870h | CAN1 Mailbox 7: Message Identifier | C1MB7 | XXXX XXXXh |
| 047871h | | | |
| 047872h | | | |
| 047873h | | | |
| 047874h | | | |
| 047875h | CAN1 Mailbox 7: Data Length | | XXh |
| 047876h | CAN1 Mailbox 7: Data Field | | XXXX XXXX XXXX XXXXh |
| 047877h | | | |
| 047878h | | | |
| 047879h | | | |
| 04787Ah | | | |
| 04787Bh | | | |
| 04787Ch | | | |
| 04787Dh | | | |
| 04787Eh | | | |
| 04787Fh | | | |
| 047880h | CAN1 Mailbox 8: Message Identifier | C1MB8 | XXXX XXXXh |
| 047881h | | | |
| 047882h | | | |
| 047883h | | | |
| 047884h | | | |
| 047885h | CAN1 Mailbox 8: Data Length | | XXh |
| 047886h | CAN1 Mailbox 8: Data Field | | XXXX XXXX XXXX XXXXh |
| 047887h | | | |
| 047888h | | | |
| 047889h | | | |
| 04788Ah | | | |
| 04788Bh | | | |
| 04788Ch | | | |
| 04788Dh | | | |
| 04788Eh | | | |
| 04788Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.31 SFR List (31)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047890h | CAN1 Mailbox 9: Message Identifier | C1MB9 | XXXX XXXXh |
| 047891h | | | |
| 047892h | | | |
| 047893h | | | |
| 047894h | | | |
| 047895h | CAN1 Mailbox 9: Data Length | | XXh |
| 047896h | CAN1 Mailbox 9: Data Field | | XXXX XXXX XXXX XXXXh |
| 047897h | | | |
| 047898h | | | |
| 047899h | | | |
| 04789Ah | | | |
| 04789Bh | | | |
| 04789Ch | | | |
| 04789Dh | | | |
| 04789Eh | CAN1 Mailbox 9: Time Stamp | | XXXXh |
| 04789Fh | | | |
| 0478A0h | CAN1 Mailbox 10: Message Identifier | C1MB10 | XXXX XXXXh |
| 0478A1h | | | |
| 0478A2h | | | |
| 0478A3h | | | |
| 0478A4h | | | |
| 0478A5h | CAN1 Mailbox 10: Data Length | | XXh |
| 0478A6h | CAN1 Mailbox 10: Data Field | | XXXX XXXX XXXX XXXXh |
| 0478A7h | | | |
| 0478A8h | | | |
| 0478A9h | | | |
| 0478AAh | | | |
| 0478ABh | | | |
| 0478ACh | | | |
| 0478ADh | | | |
| 0478AEh | CAN1 Mailbox 10: Time Stamp | | XXXXh |
| 0478AFh | | | |
| 0478B0h | CAN1 Mailbox 11: Message Identifier | C1MB11 | XXXX XXXXh |
| 0478B1h | | | |
| 0478B2h | | | |
| 0478B3h | | | |
| 0478B4h | | | |
| 0478B5h | CAN1 Mailbox 11: Data Length | | XXh |
| 0478B6h | CAN1 Mailbox 11: Data Field | | XXXX XXXX XXXX XXXXh |
| 0478B7h | | | |
| 0478B8h | | | |
| 0478B9h | | | |
| 0478BAh | | | |
| 0478BBh | | | |
| 0478BCh | | | |
| 0478BDh | | | |
| 0478BEh | CAN1 Mailbox 11: Time Stamp | | XXXXh |
| 0478BFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.32 SFR List (32)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 0478C0h | CAN1 Mailbox 12: Message Identifier | C1MB12 | XXXX XXXXh |
| 0478C1h | | | |
| 0478C2h | | | |
| 0478C3h | | | |
| 0478C4h | | | |
| 0478C5h | CAN1 Mailbox 12: Data Length | | XXh |
| 0478C6h | CAN1 Mailbox 12: Data Field | | XXXX XXXX XXXX XXXXh |
| 0478C7h | | | |
| 0478C8h | | | |
| 0478C9h | | | |
| 0478CAh | | | |
| 0478CBh | | | |
| 0478CCh | | | |
| 0478CDh | | | |
| 0478CEh | CAN1 Mailbox 12: Time Stamp | | XXXXh |
| 0478CFh | | | |
| 0478D0h | CAN1 Mailbox 13: Message Identifier | C1MB13 | XXXX XXXXh |
| 0478D1h | | | |
| 0478D2h | | | |
| 0478D3h | | | |
| 0478D4h | | | |
| 0478D5h | CAN1 Mailbox 13: Data Length | | XXh |
| 0478D6h | CAN1 Mailbox 13: Data Field | | XXXX XXXX XXXX XXXXh |
| 0478D7h | | | |
| 0478D8h | | | |
| 0478D9h | | | |
| 0478DAh | | | |
| 0478DBh | | | |
| 0478DCh | | | |
| 0478DDh | | | |
| 0478DEh | CAN1 Mailbox 13: Time Stamp | | XXXXh |
| 0478DFh | | | |
| 0478E0h | CAN1 Mailbox 14: Message Identifier | C1MB14 | XXXX XXXXh |
| 0478E1h | | | |
| 0478E2h | | | |
| 0478E3h | | | |
| 0478E4h | | | |
| 0478E5h | CAN1 Mailbox 14: Data Length | | XXh |
| 0478E6h | CAN1 Mailbox 14: Data Field | | XXXX XXXX XXXX XXXXh |
| 0478E7h | | | |
| 0478E8h | | | |
| 0478E9h | | | |
| 0478EAh | | | |
| 0478EBh | | | |
| 0478ECh | | | |
| 0478EDh | | | |
| 0478EEh | CAN1 Mailbox 14: Time Stamp | | XXXXh |
| 0478EFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.33 SFR List (33)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 0478F0h | CAN1 Mailbox 15: Message Identifier | C1MB15 | XXXX XXXXh |
| 0478F1h | | | |
| 0478F2h | | | |
| 0478F3h | | | |
| 0478F4h | | | |
| 0478F5h | CAN1 Mailbox 15: Data Length | | XXh |
| 0478F6h | CAN1 Mailbox 15: Data Field | | XXXX XXXX XXXX XXXXh |
| 0478F7h | | | |
| 0478F8h | | | |
| 0478F9h | | | |
| 0478FAh | | | |
| 0478FBh | | | |
| 0478FCh | | | |
| 0478FDh | | | |
| 0478FEh | CAN1 Mailbox 15: Time Stamp | | XXXXh |
| 0478FFh | | | |
| 047900h | CAN1 Mailbox 16: Message Identifier | C1MB16 | XXXX XXXXh |
| 047901h | | | |
| 047902h | | | |
| 047903h | | | |
| 047904h | | | |
| 047905h | CAN1 Mailbox 16: Data Length | | XXh |
| 047906h | CAN1 Mailbox 16: Data Field | | XXXX XXXX XXXX XXXXh |
| 047907h | | | |
| 047908h | | | |
| 047909h | | | |
| 04790Ah | | | |
| 04790Bh | | | |
| 04790Ch | | | |
| 04790Dh | | | |
| 04790Eh | CAN1 Mailbox 16: Time Stamp | | XXXXh |
| 04790Fh | | | |
| 047910h | CAN1 Mailbox 17: Message Identifier | C1MB17 | XXXX XXXXh |
| 047911h | | | |
| 047912h | | | |
| 047913h | | | |
| 047914h | | | |
| 047915h | CAN1 Mailbox 17: Data Length | | XXh |
| 047916h | CAN1 Mailbox 17: Data Field | | XXXX XXXX XXXX XXXXh |
| 047917h | | | |
| 047918h | | | |
| 047919h | | | |
| 04791Ah | | | |
| 04791Bh | | | |
| 04791Ch | | | |
| 04791Dh | | | |
| 04791Eh | CAN1 Mailbox 17: Time Stamp | | XXXXh |
| 04791Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.34 SFR List (34)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047920h | CAN1 Mailbox 18: Message Identifier | C1MB18 | XXXX XXXXh |
| 047921h | | | |
| 047922h | | | |
| 047923h | | | |
| 047924h | | | |
| 047925h | CAN1 Mailbox 18: Data Length | | XXh |
| 047926h | CAN1 Mailbox 18: Data Field | | XXXX XXXX XXXX XXXXh |
| 047927h | | | |
| 047928h | | | |
| 047929h | | | |
| 04792Ah | | | |
| 04792Bh | | | |
| 04792Ch | | | |
| 04792Dh | | | |
| 04792Eh | CAN1 Mailbox18: Time Stamp | | XXXXh |
| 04792Fh | | | |
| 047930h | CAN1 Mailbox 19: Message Identifier | C1MB19 | XXXX XXXXh |
| 047931h | | | |
| 047932h | | | |
| 047933h | | | |
| 047934h | | | |
| 047935h | CAN1 Mailbox 19: Data Length | | XXh |
| 047936h | CAN1 Mailbox 19: Data Field | | XXXX XXXX XXXX XXXXh |
| 047937h | | | |
| 047938h | | | |
| 047939h | | | |
| 04793Ah | | | |
| 04793Bh | | | |
| 04793Ch | | | |
| 04793Dh | | | |
| 04793Eh | CAN1 Mailbox 19: Time Stamp | | XXXXh |
| 04793Fh | | | |
| 047940h | CAN1 Mailbox 20: Message Identifier | C1MB20 | XXXX XXXXh |
| 047941h | | | |
| 047942h | | | |
| 047943h | | | |
| 047944h | | | |
| 047945h | CAN1 Mailbox 20: Data Length | | XXh |
| 047946h | CAN1 Mailbox 20: Data Field | | XXXX XXXX XXXX XXXXh |
| 047947h | | | |
| 047948h | | | |
| 047949h | | | |
| 04794Ah | | | |
| 04794Bh | | | |
| 04794Ch | | | |
| 04794Dh | | | |
| 04794Eh | CAN1 Mailbox 20: Time Stamp | | XXXXh |
| 04794Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.35 SFR List (35)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047950h | CAN1 Mailbox 21: Message Identifier | C1MB21 | XXXX XXXXh |
| 047951h | | | |
| 047952h | | | |
| 047953h | | | |
| 047954h | | | |
| 047955h | CAN1 Mailbox 21: Data Length | | XXh |
| 047956h | CAN1 Mailbox 21: Data Field | | XXXX XXXX XXXX XXXXh |
| 047957h | | | |
| 047958h | | | |
| 047959h | | | |
| 04795Ah | | | |
| 04795Bh | | | |
| 04795Ch | | | |
| 04795Dh | | | |
| 04795Eh | | | |
| 04795Fh | CAN1 Mailbox 21: Time Stamp | | XXXXh |
| 047960h | CAN1 Mailbox 22: Identifier | C1MB22 | XXXX XXXXh |
| 047961h | | | |
| 047962h | | | |
| 047963h | | | |
| 047964h | | | |
| 047965h | CAN1 Mailbox 22: Data Length | | XXh |
| 047966h | CAN1 Mailbox 22: Data Field | | XXXX XXXX XXXX XXXXh |
| 047967h | | | |
| 047968h | | | |
| 047969h | | | |
| 04796Ah | | | |
| 04796Bh | | | |
| 04796Ch | | | |
| 04796Dh | | | |
| 04796Eh | | | |
| 04796Fh | CAN1 Mailbox 22: Time Stamp | | XXXXh |
| 047970h | CAN1 Mailbox 23: Message Identifier | C1MB23 | XXXX XXXXh |
| 047971h | | | |
| 047972h | | | |
| 047973h | | | |
| 047974h | | | |
| 047975h | CAN1 Mailbox 23: Data Length | | XXh |
| 047976h | CAN1 Mailbox 23: Data Field | | XXXX XXXX XXXX XXXXh |
| 047977h | | | |
| 047978h | | | |
| 047979h | | | |
| 04797Ah | | | |
| 04797Bh | | | |
| 04797Ch | | | |
| 04797Dh | | | |
| 04797Eh | | | |
| 04797Fh | CAN1 Mailbox 23: Time Stamp | | XXXXh |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.36 SFR List (36)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047980h | CAN1 Mailbox 24: Message Identifier | C1MB24 | XXXX XXXXh |
| 047981h | | | |
| 047982h | | | |
| 047983h | | | |
| 047984h | | | |
| 047985h | CAN1 Mailbox 24: Data Length | | XXh |
| 047986h | CAN1 Mailbox 24: Data Field | | XXXX XXXX XXXX XXXXh |
| 047987h | | | |
| 047988h | | | |
| 047989h | | | |
| 04798Ah | | | |
| 04798Bh | | | |
| 04798Ch | | | |
| 04798Dh | | | |
| 04798Eh | CAN1 Mailbox 24: Time Stamp | | XXXXh |
| 04798Fh | | | |
| 047990h | CAN1 Mailbox 25: Message Identifier | C1MB25 | XXXX XXXXh |
| 047991h | | | |
| 047992h | | | |
| 047993h | | | |
| 047994h | | | |
| 047995h | CAN1 Mailbox 25: Data Length | | XXh |
| 047996h | CAN1 Mailbox 25: Data Field | | XXXX XXXX XXXX XXXXh |
| 047997h | | | |
| 047998h | | | |
| 047999h | | | |
| 04799Ah | | | |
| 04799Bh | | | |
| 04799Ch | | | |
| 04799Dh | | | |
| 04799Eh | CAN1 Mailbox 25: Time Stamp | | XXXXh |
| 04799Fh | | | |
| 0479A0h | CAN1 Mailbox 26: Message Identifier | C1MB26 | XXXX XXXXh |
| 0479A1h | | | |
| 0479A2h | | | |
| 0479A3h | | | |
| 0479A4h | | | |
| 0479A5h | CAN1 Mailbox 26: Data Length | | XXh |
| 0479A6h | CAN1 Mailbox 26: Data Field | | XXXX XXXX XXXX XXXXh |
| 0479A7h | | | |
| 0479A8h | | | |
| 0479A9h | | | |
| 0479AAh | | | |
| 0479ABh | | | |
| 0479ACh | | | |
| 0479ADh | | | |
| 0479AEh | CAN1 Mailbox 26: Time Stamp | | XXXXh |
| 0479AFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.37 SFR List (37)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 0479B0h | CAN1 Mailbox 27: Message Identifier | C1MB27 | XXXX XXXXh |
| 0479B1h | | | |
| 0479B2h | | | |
| 0479B3h | | | |
| 0479B4h | | | |
| 0479B5h | CAN1 Mailbox 27: Data Length | | XXh |
| 0479B6h | CAN1 Mailbox 27: Data Field | | XXXX XXXX XXXX XXXXh |
| 0479B7h | | | |
| 0479B8h | | | |
| 0479B9h | | | |
| 0479BAh | | | |
| 0479BBh | | | |
| 0479BCh | | | |
| 0479BDh | | | |
| 0479BEh | CAN1 Mailbox 27: Time Stamp | | XXXXh |
| 0479BFh | | | |
| 0479C0h | CAN1 Mailbox 28: Message Identifier | C1MB28 | XXXX XXXXh |
| 0479C1h | | | |
| 0479C2h | | | |
| 0479C3h | | | |
| 0479C4h | | | |
| 0479C5h | CAN1 Mailbox 28: Data Length | | XXh |
| 0479C6h | CAN1 Mailbox 28: Data Field | | XXXX XXXX XXXX XXXXh |
| 0479C7h | | | |
| 0479C8h | | | |
| 0479C9h | | | |
| 0479CAh | | | |
| 0479CBh | | | |
| 0479CCh | | | |
| 0479CDh | | | |
| 0479CEh | CAN1 Mailbox 28: Time Stamp | | XXXXh |
| 0479CFh | | | |
| 0479D0h | CAN1 Mailbox 29: Message Identifier | C1MB29 | XXXX XXXXh |
| 0479D1h | | | |
| 0479D2h | | | |
| 0479D3h | | | |
| 0479D4h | | | |
| 0479D5h | CAN1 Mailbox 29: Data Length | | XXh |
| 0479D6h | CAN1 Mailbox 29: Data Field | | XXXX XXXX XXXX XXXXh |
| 0479D7h | | | |
| 0479D8h | | | |
| 0479D9h | | | |
| 0479DAh | | | |
| 0479DBh | | | |
| 0479DCh | | | |
| 0479DDh | | | |
| 0479DEh | CAN1 Mailbox 29: Time Stamp | | XXXXh |
| 0479DFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.38 SFR List (38)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 0479E0h | CAN1 Mailbox 30: Message Identifier | C1MB30 | XXXX XXXXh |
| 0479E1h | | | |
| 0479E2h | | | |
| 0479E3h | | | |
| 0479E4h | | | |
| 0479E5h | CAN1 Mailbox 30: Data Length | | XXh |
| 0479E6h | CAN1 Mailbox 30: Data Field | | XXXX XXXX XXXX XXXXh |
| 0479E7h | | | |
| 0479E8h | | | |
| 0479E9h | | | |
| 0479EAh | | | |
| 0479EBh | | | |
| 0479ECh | | | |
| 0479EDh | | | |
| 0479EEh | CAN1 Mailbox 30: Time Stamp | | XXXXh |
| 0479EFh | | | |
| 0479F0h | CAN1 Mailbox 31: Message Identifier | C1MB31 | XXXX XXXXh |
| 0479F1h | | | |
| 0479F2h | | | |
| 0479F3h | | | |
| 0479F4h | | | |
| 0479F5h | CAN1 Mailbox 31: Data Length | | XXh |
| 0479F6h | CAN1 Mailbox 31: Data Field | | XXXX XXXX XXXX XXXXh |
| 0479F7h | | | |
| 0479F8h | | | |
| 0479F9h | | | |
| 0479FAh | | | |
| 0479FBh | | | |
| 0479FCh | | | |
| 0479FDh | | | |
| 0479FEh | CAN1 Mailbox 31: Time Stamp | | XXXXh |
| 0479FFh | | | |
| 047A00h | CAN1 Acceptance Mask Register 0 | C1MKR0 | XXXX XXXXh |
| 047A01h | | | |
| 047A02h | | | |
| 047A03h | | | |
| 047A04h | CAN1 Acceptance Mask Register 1 | C1MKR1 | XXXX XXXXh |
| 047A05h | | | |
| 047A06h | | | |
| 047A07h | | | |
| 047A08h | CAN1 Acceptance Mask Register 2 | C1MKR2 | XXXX XXXXh |
| 047A09h | | | |
| 047A0Ah | | | |
| 047A0Bh | | | |
| 047A0Ch | CAN1 Acceptance Mask Register 3 | C1MKR3 | XXXX XXXXh |
| 047A0Dh | | | |
| 047A0Eh | | | |
| 047A0Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.39 SFR List (39)

| Address | Register | Symbol | Reset Value |
|-----------------------|--|----------|-------------|
| 047A10h | CAN1 Acceptance Mask Register 4 | C1MKR4 | XXXX XXXXh |
| 047A11h | | | |
| 047A12h | | | |
| 047A13h | | | |
| 047A14h | CAN1 Acceptance Mask Register 5 | C1MKR5 | XXXX XXXXh |
| 047A15h | | | |
| 047A16h | | | |
| 047A17h | | | |
| 047A18h | CAN1 Acceptance Mask Register 6 | C1MKR6 | XXXX XXXXh |
| 047A19h | | | |
| 047A1Ah | | | |
| 047A1Bh | | | |
| 047A1Ch | CAN1 Acceptance Mask Register 7 | C1MKR7 | XXXX XXXXh |
| 047A1Dh | | | |
| 047A1Eh | | | |
| 047A1Fh | | | |
| 047A20h | CAN1 FIFO Received ID Compare Register 0 | C1FIDCR0 | XXXX XXXXh |
| 047A21h | | | |
| 047A22h | | | |
| 047A23h | | | |
| 047A24h | CAN1 FIFO Received ID Compare Register 1 | C1FIDCR1 | XXXX XXXXh |
| 047A25h | | | |
| 047A26h | | | |
| 047A27h | | | |
| 047A28h | CAN1 Mask Invalid Register | C1MKIVLR | XXXX XXXXh |
| 047A29h | | | |
| 047A2Ah | | | |
| 047A2Bh | | | |
| 047A2Ch | CAN1 Mailbox Interrupt Enable Register | C1MIER | XXXX XXXXh |
| 047A2Dh | | | |
| 047A2Eh | | | |
| 047A2Fh | | | |
| 047A30h | | | |
| 047A31h | | | |
| 047A32h | | | |
| 047A33h | | | |
| 047A34h | | | |
| 047A35h | | | |
| 047A36h | | | |
| 047A37h | | | |
| 047A38h | | | |
| 047A39h | | | |
| 047A3Ah | | | |
| 047A3Bh | | | |
| 047A3Ch | | | |
| 047A3Dh | | | |
| 047A3Eh | | | |
| 047A3Fh | | | |
| 047A40h to 047B1Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.40 SFR List (40)

| Address | Register | Symbol | Reset Value |
|---------|----------------------------------|----------|-------------|
| 047B20h | CAN1 Message Control Register 0 | C1MCTL0 | 00h |
| 047B21h | CAN1 Message Control Register 1 | C1MCTL1 | 00h |
| 047B22h | CAN1 Message Control Register 2 | C1MCTL2 | 00h |
| 047B23h | CAN1 Message Control Register 3 | C1MCTL3 | 00h |
| 047B24h | CAN1 Message Control Register 4 | C1MCTL4 | 00h |
| 047B25h | CAN1 Message Control Register 5 | C1MCTL5 | 00h |
| 047B26h | CAN1 Message Control Register 6 | C1MCTL6 | 00h |
| 047B27h | CAN1 Message Control Register 7 | C1MCTL7 | 00h |
| 047B28h | CAN1 Message Control Register 8 | C1MCTL8 | 00h |
| 047B29h | CAN1 Message Control Register 9 | C1MCTL9 | 00h |
| 047B2Ah | CAN1 Message Control Register 10 | C1MCTL10 | 00h |
| 047B2Bh | CAN1 Message Control Register 11 | C1MCTL11 | 00h |
| 047B2Ch | CAN1 Message Control Register 12 | C1MCTL12 | 00h |
| 047B2Dh | CAN1 Message Control Register 13 | C1MCTL13 | 00h |
| 047B2Eh | CAN1 Message Control Register 14 | C1MCTL14 | 00h |
| 047B2Fh | CAN1 Message Control Register 15 | C1MCTL15 | 00h |
| 047B30h | CAN1 Message Control Register 16 | C1MCTL16 | 00h |
| 047B31h | CAN1 Message Control Register 17 | C1MCTL17 | 00h |
| 047B32h | CAN1 Message Control Register 18 | C1MCTL18 | 00h |
| 047B33h | CAN1 Message Control Register 19 | C1MCTL19 | 00h |
| 047B34h | CAN1 Message Control Register 20 | C1MCTL20 | 00h |
| 047B35h | CAN1 Message Control Register 21 | C1MCTL21 | 00h |
| 047B36h | CAN1 Message Control Register 22 | C1MCTL22 | 00h |
| 047B37h | CAN1 Message Control Register 23 | C1MCTL23 | 00h |
| 047B38h | CAN1 Message Control Register 24 | C1MCTL24 | 00h |
| 047B39h | CAN1 Message Control Register 25 | C1MCTL25 | 00h |
| 047B3Ah | CAN1 Message Control Register 26 | C1MCTL26 | 00h |
| 047B3Bh | CAN1 Message Control Register 27 | C1MCTL27 | 00h |
| 047B3Ch | CAN1 Message Control Register 28 | C1MCTL28 | 00h |
| 047B3Dh | CAN1 Message Control Register 29 | C1MCTL29 | 00h |
| 047B3Eh | CAN1 Message Control Register 30 | C1MCTL30 | 00h |
| 047B3Fh | CAN1 Message Control Register 31 | C1MCTL31 | 00h |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.41 SFR List (41)

| Address | Register | Symbol | Reset Value |
|-----------------------|---|---------|-------------|
| 047B40h | CAN1 Control Register | C1CTLR | 0000 0101b |
| 047B41h | | | 0000 0000b |
| 047B42h | CAN1 Status Register | C1STR | 0000 0101b |
| 047B43h | | | 0000 0000b |
| 047B44h | CAN1 Bit Configuration Register | C1BCR | 00 0000h |
| 047B45h | | | |
| 047B46h | | | |
| 047B47h | CAN1 Clock Select Register | C1CLKR | 000X 0000b |
| 047B48h | CAN1 Receive FIFO Control Register | C1RFCR | 1000 0000b |
| 047B49h | CAN1 Receive FIFO Pointer Control Register | C1RFPCR | XXh |
| 047B4Ah | CAN1 Transmit FIFO Control Register | C1TFCR | 1000 0000b |
| 047B4Bh | CAN1 Transmit FIFO Pointer Control Register | C1TFPCR | XXh |
| 047B4Ch | CAN1 Error Interrupt Enable Register | C1EIER | 00h |
| 047B4Dh | CAN1 Error Interrupt Factor Judge Register | C1EIFR | 00h |
| 047B4Eh | CAN1 Receive Error Count Register | C1RECR | 00h |
| 047B4Fh | CAN1 Transmit Error Count Register | C1TECR | 00h |
| 047B50h | CAN1 Error Code Store Register | C1ECSR | 00h |
| 047B51h | CAN1 Channel Search Support Register | C1CSSR | XXh |
| 047B52h | CAN1 Mailbox Search Status Register | C1MSSR | 1000 0000b |
| 047B53h | CAN1 Mailbox Search Mode Register | C1MSMR | XXXX XX00b |
| 047B54h | CAN1 Time Stamp Register | C1TSR | 0000h |
| 047B55h | | | |
| 047B56h | CAN1 Acceptance Filter Support Register | C1AFSR | XXXXh |
| 047B57h | | | |
| 047B58h | CAN1 Test Control Register | C1TCR | 00h |
| 047B59h | | | |
| 047B5Ah | | | |
| 047B5Bh | | | |
| 047B5Ch | | | |
| 047B5Dh | | | |
| 047B5Eh | | | |
| 047B5Fh | | | |
| 047B60h to 047BFFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.42 SFR List (42)

| Address | Register | Symbol | Reset Value |
|---------|------------------------------------|--------|-------------------------|
| 047C00h | CAN0 Mailbox 0: Message Identifier | COMB0 | XXXX XXXXh |
| 047C01h | | | |
| 047C02h | | | |
| 047C03h | | | |
| 047C04h | | | |
| 047C05h | CAN0 Mailbox 0: Data Length | | XXh |
| 047C06h | CAN0 Mailbox 0: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C07h | | | |
| 047C08h | | | |
| 047C09h | | | |
| 047C0Ah | | | |
| 047C0Bh | | | |
| 047C0Ch | | | |
| 047C0Dh | | | |
| 047C0Eh | | | |
| 047C0Fh | | | |
| 047C10h | CAN0 Mailbox 1: Message Identifier | COMB1 | XXXX XXXXh |
| 047C11h | | | |
| 047C12h | | | |
| 047C13h | | | |
| 047C14h | | | |
| 047C15h | CAN0 Mailbox 1: Data Length | | XXh |
| 047C16h | CAN0 Mailbox 1: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C17h | | | |
| 047C18h | | | |
| 047C19h | | | |
| 047C1Ah | | | |
| 047C1Bh | | | |
| 047C1Ch | | | |
| 047C1Dh | | | |
| 047C1Eh | | | |
| 047C1Fh | | | |
| 047C20h | CAN0 Mailbox 2: Message Identifier | COMB2 | XXXX XXXXh |
| 047C21h | | | |
| 047C22h | | | |
| 047C23h | | | |
| 047C24h | | | |
| 047C25h | CAN0 Mailbox 2: Data Length | | XXh |
| 047C26h | CAN0 Mailbox 2: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C27h | | | |
| 047C28h | | | |
| 047C29h | | | |
| 047C2Ah | | | |
| 047C2Bh | | | |
| 047C2Ch | | | |
| 047C2Dh | | | |
| 047C2Eh | | | |
| 047C2Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.43 SFR List (43)

| Address | Register | Symbol | Reset Value |
|---------|------------------------------------|--------|-------------------------|
| 047C30h | CAN0 Mailbox 3: Message Identifier | COMB3 | XXXX XXXXh |
| 047C31h | | | |
| 047C32h | | | |
| 047C33h | | | |
| 047C34h | | | |
| 047C35h | CAN0 Mailbox 3: Data Length | | XXh |
| 047C36h | CAN0 Mailbox 3: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C37h | | | |
| 047C38h | | | |
| 047C39h | | | |
| 047C3Ah | | | |
| 047C3Bh | | | |
| 047C3Ch | | | |
| 047C3Dh | | | |
| 047C3Eh | CAN0 Mailbox 3: Time Stamp | | XXXXh |
| 047C3Fh | | | |
| 047C40h | CAN0 Mailbox 4: Message Identifier | COMB4 | XXXX XXXXh |
| 047C41h | | | |
| 047C42h | | | |
| 047C43h | | | |
| 047C44h | | | |
| 047C45h | CAN0 Mailbox 4: Data Length | | XXh |
| 047C46h | CAN0 Mailbox 4: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C47h | | | |
| 047C48h | | | |
| 047C49h | | | |
| 047C4Ah | | | |
| 047C4Bh | | | |
| 047C4Ch | | | |
| 047C4Dh | | | |
| 047C4Eh | CAN0 Mailbox 4: Time Stamp | | XXXXh |
| 047C4Fh | | | |
| 047C50h | CAN0 Mailbox 5: Message Identifier | COMB5 | XXXX XXXXh |
| 047C51h | | | |
| 047C52h | | | |
| 047C53h | | | |
| 047C54h | | | |
| 047C55h | CAN0 Mailbox 5: Data Length | | XXh |
| 047C56h | CAN0 Mailbox 5: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C57h | | | |
| 047C58h | | | |
| 047C59h | | | |
| 047C5Ah | | | |
| 047C5Bh | | | |
| 047C5Ch | | | |
| 047C5Dh | | | |
| 047C5Eh | CAN0 Mailbox 5: Time Stamp | | XXXXh |
| 047C5Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.44 SFR List (44)

| Address | Register | Symbol | Reset Value |
|---------|------------------------------------|--------|-------------------------|
| 047C60h | CAN0 Mailbox 6: Message Identifier | COMB6 | XXXX XXXXh |
| 047C61h | | | |
| 047C62h | | | |
| 047C63h | | | |
| 047C64h | | | |
| 047C65h | CAN0 Mailbox 6: Data Length | | XXh |
| 047C66h | CAN0 Mailbox 6: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C67h | | | |
| 047C68h | | | |
| 047C69h | | | |
| 047C6Ah | | | |
| 047C6Bh | | | |
| 047C6Ch | | | |
| 047C6Dh | | | |
| 047C6Eh | CAN0 Mailbox 6: Time Stamp | | XXXXh |
| 047C6Fh | | | |
| 047C70h | CAN0 Mailbox 7: Message Identifier | COMB7 | XXXX XXXXh |
| 047C71h | | | |
| 047C72h | | | |
| 047C73h | | | |
| 047C74h | | | |
| 047C75h | CAN0 Mailbox 7: Data Length | | XXh |
| 047C76h | CAN0 Mailbox 7: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C77h | | | |
| 047C78h | | | |
| 047C79h | | | |
| 047C7Ah | | | |
| 047C7Bh | | | |
| 047C7Ch | | | |
| 047C7Dh | | | |
| 047C7Eh | CAN0 Mailbox 7: Time Stamp | | XXXXh |
| 047C7Fh | | | |
| 047C80h | CAN0 Mailbox 8: Message Identifier | COMB8 | XXXX XXXXh |
| 047C81h | | | |
| 047C82h | | | |
| 047C83h | | | |
| 047C84h | | | |
| 047C85h | CAN0 Mailbox 8: Data Length | | XXh |
| 047C86h | CAN0 Mailbox 8: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C87h | | | |
| 047C88h | | | |
| 047C89h | | | |
| 047C8Ah | | | |
| 047C8Bh | | | |
| 047C8Ch | | | |
| 047C8Dh | | | |
| 047C8Eh | CAN0 Mailbox 8: Time Stamp | | XXXXh |
| 047C8Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.45 SFR List (45)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047C90h | CAN0 Mailbox 9: Message Identifier | COMB9 | XXXX XXXXh |
| 047C91h | | | |
| 047C92h | | | |
| 047C93h | | | |
| 047C94h | | | |
| 047C95h | CAN0 Mailbox 9: Data Length | | XXh |
| 047C96h | CAN0 Mailbox 9: Data Field | | XXXX XXXX XXXX XXXXh |
| 047C97h | | | |
| 047C98h | | | |
| 047C99h | | | |
| 047C9Ah | | | |
| 047C9Bh | | | |
| 047C9Ch | | | |
| 047C9Dh | | | |
| 047C9Eh | CAN0 Mailbox 9: Time Stamp | | XXXXh |
| 047C9Fh | | | |
| 047CA0h | CAN0 Mailbox 10: Message Identifier | COMB10 | XXXX XXXXh |
| 047CA1h | | | |
| 047CA2h | | | |
| 047CA3h | | | |
| 047CA4h | | | |
| 047CA5h | CAN0 Mailbox 10: Data Length | | XXh |
| 047CA6h | CAN0 Mailbox 10: Data Field | | XXXX XXXX XXXX XXXXh |
| 047CA7h | | | |
| 047CA8h | | | |
| 047CA9h | | | |
| 047CAAh | | | |
| 047CABh | | | |
| 047CACh | | | |
| 047CADh | | | |
| 047CAEh | CAN0 Mailbox 10: Time Stamp | | XXXXh |
| 047CAFh | | | |
| 047CB0h | CAN0 Mailbox 11: Message Identifier | COMB11 | XXXX XXXXh |
| 047CB1h | | | |
| 047CB2h | | | |
| 047CB3h | | | |
| 047CB4h | | | |
| 047CB5h | CAN0 Mailbox 11: Data Length | | XXh |
| 047CB6h | CAN0 Mailbox 11: Data Field | | XXXX XXXX XXXX XXXXh |
| 047CB7h | | | |
| 047CB8h | | | |
| 047CB9h | | | |
| 047CBAh | | | |
| 047CBBh | | | |
| 047CBCh | | | |
| 047CBDh | | | |
| 047CBEh | CAN0 Mailbox 11: Time Stamp | | XXXXh |
| 047CBFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.46 SFR List (46)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047CC0h | CAN0 Mailbox 12: Message Identifier | C0MB12 | XXXX XXXXh |
| 047CC1h | | | |
| 047CC2h | | | |
| 047CC3h | | | |
| 047CC4h | | | |
| 047CC5h | CAN0 Mailbox 12: Data Length | | XXh |
| 047CC6h | CAN0 Mailbox 12: Data Field | | XXXX XXXX XXXX XXXXh |
| 047CC7h | | | |
| 047CC8h | | | |
| 047CC9h | | | |
| 047CCAh | | | |
| 047CCBh | | | |
| 047CCCh | | | |
| 047CCDh | | | |
| 047CCEh | | | |
| 047CCFh | | | |
| 047CD0h | CAN0 Mailbox 13: Message Identifier | C0MB13 | XXXX XXXXh |
| 047CD1h | | | |
| 047CD2h | | | |
| 047CD3h | | | |
| 047CD4h | | | |
| 047CD5h | CAN0 Mailbox 13: Data Length | | XXh |
| 047CD6h | CAN0 Mailbox 13: Data Field | | XXXX XXXX XXXX XXXXh |
| 047CD7h | | | |
| 047CD8h | | | |
| 047CD9h | | | |
| 047CDAh | | | |
| 047CDBh | | | |
| 047CDCh | | | |
| 047CDDh | | | |
| 047CDEh | | | |
| 047CDFh | | | |
| 047CE0h | CAN0 Mailbox 14: Message Identifier | C0MB14 | XXXX XXXXh |
| 047CE1h | | | |
| 047CE2h | | | |
| 047CE3h | | | |
| 047CE4h | | | |
| 047CE5h | CAN0 Mailbox 14: Data Length | | XXh |
| 047CE6h | CAN0 Mailbox 14: Data Field | | XXXX XXXX XXXX XXXXh |
| 047CE7h | | | |
| 047CE8h | | | |
| 047CE9h | | | |
| 047CEAh | | | |
| 047CEBh | | | |
| 047CECh | | | |
| 047CEDh | | | |
| 047CEEh | | | |
| 047CEFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.47 SFR List (47)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047CF0h | CAN0 Mailbox 15: Message Identifier | C0MB15 | XXXX XXXXh |
| 047CF1h | | | |
| 047CF2h | | | |
| 047CF3h | | | |
| 047CF4h | | | |
| 047CF5h | CAN0 Mailbox 15: Data Length | | XXh |
| 047CF6h | CAN0 Mailbox 15: Data Field | | XXXX XXXX XXXX XXXXh |
| 047CF7h | | | |
| 047CF8h | | | |
| 047CF9h | | | |
| 047CFAh | | | |
| 047CFBh | | | |
| 047CFCh | | | |
| 047CFDh | | | |
| 047CFEh | CAN0 Mailbox 15: Time Stamp | | XXXXh |
| 047CFFh | | | |
| 047D00h | CAN0 Mailbox 16: Message Identifier | C0MB16 | XXXX XXXXh |
| 047D01h | | | |
| 047D02h | | | |
| 047D03h | | | |
| 047D04h | | | |
| 047D05h | CAN0 Mailbox 16: Data Length | | XXh |
| 047D06h | CAN0 Mailbox 16: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D07h | | | |
| 047D08h | | | |
| 047D09h | | | |
| 047D0Ah | | | |
| 047D0Bh | | | |
| 047D0Ch | | | |
| 047D0Dh | | | |
| 047D0Eh | CAN0 Mailbox 16: Time Stamp | | XXXXh |
| 047D0Fh | | | |
| 047D10h | CAN0 Mailbox 17: Message Identifier | C0MB17 | XXXX XXXXh |
| 047D11h | | | |
| 047D12h | | | |
| 047D13h | | | |
| 047D14h | | | |
| 047D15h | CAN0 Mailbox 17: Data Length | | XXh |
| 047D16h | CAN0 Mailbox 17: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D17h | | | |
| 047D18h | | | |
| 047D19h | | | |
| 047D1Ah | | | |
| 047D1Bh | | | |
| 047D1Ch | | | |
| 047D1Dh | | | |
| 047D1Eh | CAN0 Mailbox 17: Time Stamp | | XXXXh |
| 047D1Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.48 SFR List (48)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047D20h | CAN0 Mailbox 18: Message Identifier | C0MB18 | XXXX XXXXh |
| 047D21h | | | |
| 047D22h | | | |
| 047D23h | | | |
| 047D24h | | | |
| 047D25h | CAN0 Mailbox 18: Data Length | | XXh |
| 047D26h | CAN0 Mailbox 18: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D27h | | | |
| 047D28h | | | |
| 047D29h | | | |
| 047D2Ah | | | |
| 047D2Bh | | | |
| 047D2Ch | | | |
| 047D2Dh | | | |
| 047D2Eh | CAN0 Mailbox 18: Time Stamp | | XXXXh |
| 047D2Fh | | | |
| 047D30h | CAN0 Mailbox 19: Message Identifier | C0MB19 | XXXX XXXXh |
| 047D31h | | | |
| 047D32h | | | |
| 047D33h | | | |
| 047D34h | | | |
| 047D35h | CAN0 Mailbox 19: Data Length | | XXh |
| 047D36h | CAN0 Mailbox 19: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D37h | | | |
| 047D38h | | | |
| 047D39h | | | |
| 047D3Ah | | | |
| 047D3Bh | | | |
| 047D3Ch | | | |
| 047D3Dh | | | |
| 047D3Eh | CAN0 Mailbox 19: Time Stamp | | XXXXh |
| 047D3Fh | | | |
| 047D40h | CAN0 Mailbox 20: Message Identifier | C0MB20 | XXXX XXXXh |
| 047D41h | | | |
| 047D42h | | | |
| 047D43h | | | |
| 047D44h | | | |
| 047D45h | CAN0 Mailbox 20: Data Length | | XXh |
| 047D46h | CAN0 Mailbox 20: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D47h | | | |
| 047D48h | | | |
| 047D49h | | | |
| 047D4Ah | | | |
| 047D4Bh | | | |
| 047D4Ch | | | |
| 047D4Dh | | | |
| 047D4Eh | CAN0 Mailbox 20: Time Stamp | | XXXXh |
| 047D4Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.49 SFR List (49)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047D50h | CAN0 Mailbox 21: Message Identifier | C0MB21 | XXXX XXXXh |
| 047D51h | | | |
| 047D52h | | | |
| 047D53h | | | |
| 047D54h | | | |
| 047D55h | CAN0 Mailbox 21: Data Length | | XXh |
| 047D56h | CAN0 Mailbox 21: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D57h | | | |
| 047D58h | | | |
| 047D59h | | | |
| 047D5Ah | | | |
| 047D5Bh | | | |
| 047D5Ch | | | |
| 047D5Dh | | | |
| 047D5Eh | CAN0 Mailbox 21: Time Stamp | | XXXXh |
| 047D5Fh | | | |
| 047D60h | CAN0 Mailbox 22: Message Identifier | C0MB22 | XXXX XXXXh |
| 047D61h | | | |
| 047D62h | | | |
| 047D63h | | | |
| 047D64h | | | |
| 047D65h | CAN0 Mailbox 22: Data Length | | XXh |
| 047D66h | CAN0 Mailbox 22: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D67h | | | |
| 047D68h | | | |
| 047D69h | | | |
| 047D6Ah | | | |
| 047D6Bh | | | |
| 047D6Ch | | | |
| 047D6Dh | | | |
| 047D6Eh | CAN0 Mailbox 22: Time Stamp | | XXXXh |
| 047D6Fh | | | |
| 047D70h | CAN0 Mailbox 23: Message Identifier | C0MB23 | XXXX XXXXh |
| 047D71h | | | |
| 047D72h | | | |
| 047D73h | | | |
| 047D74h | | | |
| 047D75h | CAN0 Mailbox 23: Data Length | | XXh |
| 047D76h | CAN0 Mailbox 23: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D77h | | | |
| 047D78h | | | |
| 047D79h | | | |
| 047D7Ah | | | |
| 047D7Bh | | | |
| 047D7Ch | | | |
| 047D7Dh | | | |
| 047D7Eh | CAN0 Mailbox 23: Time Stamp | | XXXXh |
| 047D7Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.50 SFR List (50)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047D80h | CAN0 Mailbox 24: Message Identifier | C0MB24 | XXXX XXXXh |
| 047D81h | | | |
| 047D82h | | | |
| 047D83h | | | |
| 047D84h | | | |
| 047D85h | CAN0 Mailbox 24: Data Length | | XXh |
| 047D86h | CAN0 Mailbox 24: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D87h | | | |
| 047D88h | | | |
| 047D89h | | | |
| 047D8Ah | | | |
| 047D8Bh | | | |
| 047D8Ch | | | |
| 047D8Dh | | | |
| 047D8Eh | CAN0 Mailbox 24: Time Stamp | | XXXXh |
| 047D8Fh | | | |
| 047D90h | CAN0 Mailbox 25: Message Identifier | C0MB25 | XXXX XXXXh |
| 047D91h | | | |
| 047D92h | | | |
| 047D93h | | | |
| 047D94h | | | |
| 047D95h | CAN0 Mailbox 25: Data Length | | XXh |
| 047D96h | CAN0 Mailbox 25: Data Field | | XXXX XXXX XXXX XXXXh |
| 047D97h | | | |
| 047D98h | | | |
| 047D99h | | | |
| 047D9Ah | | | |
| 047D9Bh | | | |
| 047D9Ch | | | |
| 047D9Dh | | | |
| 047D9Eh | CAN0 Mailbox 25: Time Stamp | | XXXXh |
| 047D9Fh | | | |
| 047DA0h | CAN0 Mailbox 26: Message Identifier | C0MB26 | XXXX XXXXh |
| 047DA1h | | | |
| 047DA2h | | | |
| 047DA3h | | | |
| 047DA4h | | | |
| 047DA5h | CAN0 Mailbox 26: Data Length | | XXh |
| 047DA6h | CAN0 Mailbox 26: Data Field | | XXXX XXXX XXXX XXXXh |
| 047DA7h | | | |
| 047DA8h | | | |
| 047DA9h | | | |
| 047DAAh | | | |
| 047DABh | | | |
| 047DACH | | | |
| 047DADh | | | |
| 047DAEh | CAN0 Mailbox 26: Time Stamp | | XXXXh |
| 047DAFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.51 SFR List (51)

| Address | Register | Symbol | Reset Value |
|----------|-------------------------------------|--------|-------------------------|
| 047DB0h | CAN0 Mailbox 27: Message Identifier | C0MB27 | XXXX XXXXh |
| 047DB1h | | | |
| 047DB2h | | | |
| 047DB3h | | | |
| 047DB4h | | | |
| 047DB5h | CAN0 Mailbox 27: Data Length | | XXh |
| 047DB6h | CAN0 Mailbox 27: Data Field | | XXXX XXXX XXXX XXXXh |
| 047DB7h | | | |
| 047DB8h | | | |
| 047DB9h | | | |
| 047DBAh | | | |
| 047DBBh | | | |
| 047DBCCh | | | |
| 047DBDh | | | |
| 047DBEh | | | |
| 047DBFh | | | |
| 047DC0h | CAN0 Mailbox 28: Message Identifier | C0MB28 | XXXX XXXXh |
| 047DC1h | | | |
| 047DC2h | | | |
| 047DC3h | | | |
| 047DC4h | | | |
| 047DC5h | CAN0 Mailbox 28: Data Length | | XXh |
| 047DC6h | CAN0 Mailbox 28: Data Field | | XXXX XXXX XXXX XXXXh |
| 047DC7h | | | |
| 047DC8h | | | |
| 047DC9h | | | |
| 047DCAh | | | |
| 047DCBh | | | |
| 047DCCCh | | | |
| 047DCDh | | | |
| 047DCEh | | | |
| 047DCFh | | | |
| 047DD0h | CAN0 Mailbox 29: Message Identifier | C0MB29 | XXXX XXXXh |
| 047DD1h | | | |
| 047DD2h | | | |
| 047DD3h | | | |
| 047DD4h | | | |
| 047DD5h | CAN0 Mailbox 29: Data Length | | XXh |
| 047DD6h | CAN0 Mailbox 29: Data Field | | XXXX XXXX XXXX XXXXh |
| 047DD7h | | | |
| 047DD8h | | | |
| 047DD9h | | | |
| 047DDAh | | | |
| 047DDBh | | | |
| 047DDCCh | | | |
| 047DDDh | | | |
| 047DDEh | | | |
| 047DDFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.52 SFR List (52)

| Address | Register | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------------------|
| 047DE0h | CAN0 Mailbox 30: Message Identifier | COMB30 | XXXX XXXXh |
| 047DE1h | | | |
| 047DE2h | | | |
| 047DE3h | | | |
| 047DE4h | | | |
| 047DE5h | CAN0 Mailbox 30: Data Length | | XXh |
| 047DE6h | CAN0 Mailbox 30: Data Field | | XXXX XXXX XXXX XXXXh |
| 047DE7h | | | |
| 047DE8h | | | |
| 047DE9h | | | |
| 047DEAh | | | |
| 047DEBh | | | |
| 047DECh | | | |
| 047DEDh | | | |
| 047DEEh | CAN0 Mailbox 30: Time Stamp | | XXXXh |
| 047DEFh | | | |
| 047DF0h | CAN0 Mailbox 31: Message Identifier | COMB31 | XXXX XXXXh |
| 047DF1h | | | |
| 047DF2h | | | |
| 047DF3h | | | |
| 047DF4h | | | |
| 047DF5h | CAN0 Mailbox 31: Data Length | | XXh |
| 047DF6h | CAN0 Mailbox 31: Data Field | | XXXX XXXX XXXX XXXXh |
| 047DF7h | | | |
| 047DF8h | | | |
| 047DF9h | | | |
| 047DFAh | | | |
| 047DFBh | | | |
| 047DFCh | | | |
| 047DFDh | | | |
| 047DFEh | CAN0 Mailbox 31: Time Stamp | | XXXXh |
| 047DFFh | | | |
| 047E00h | CAN0 Acceptance Mask Register 0 | COMKR0 | XXXX XXXXh |
| 047E01h | | | |
| 047E02h | | | |
| 047E03h | | | |
| 047E04h | CAN0 Acceptance Mask Register 1 | COMKR1 | XXXX XXXXh |
| 047E05h | | | |
| 047E06h | | | |
| 047E07h | | | |
| 047E08h | CAN0 Acceptance Mask Register 2 | COMKR2 | XXXX XXXXh |
| 047E09h | | | |
| 047E0Ah | | | |
| 047E0Bh | | | |
| 047E0Ch | CAN0 Acceptance Mask Register 3 | COMKR3 | XXXX XXXXh |
| 047E0Dh | | | |
| 047E0Eh | | | |
| 047E0Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.53 SFR List (53)

| Address | Register | Symbol | Reset Value |
|-----------------------|---|----------|-------------|
| 047E10h | CAN0 Acceptance Mask Register 4 | COMKR4 | XXXX XXXXh |
| 047E11h | | | |
| 047E12h | | | |
| 047E13h | | | |
| 047E14h | CAN0 Acceptance Mask Register 5 | COMKR5 | XXXX XXXXh |
| 047E15h | | | |
| 047E16h | | | |
| 047E17h | | | |
| 047E18h | CAN0 Acceptance Mask Register 6 | COMKR6 | XXXX XXXXh |
| 047E19h | | | |
| 047E1Ah | | | |
| 047E1Bh | | | |
| 047E1Ch | CAN0 Acceptance Mask Register 7 | COMKR7 | XXXX XXXXh |
| 047E1Dh | | | |
| 047E1Eh | | | |
| 047E1Fh | | | |
| 047E20h | CAN0 FIFO Receive ID Compare Register 0 | C0FIDCR0 | XXXX XXXXh |
| 047E21h | | | |
| 047E22h | | | |
| 047E23h | | | |
| 047E24h | CAN0 FIFO Receive ID Compare Register 1 | C0FIDCR1 | XXXX XXXXh |
| 047E25h | | | |
| 047E26h | | | |
| 047E27h | | | |
| 047E28h | CAN0 Mask Invalid Register | COMKIVLR | XXXX XXXXh |
| 047E29h | | | |
| 047E2Ah | | | |
| 047E2Bh | | | |
| 047E2Ch | CAN0 Mailbox Interrupt Enable Register | COMIER | XXXX XXXXh |
| 047E2Dh | | | |
| 047E2Eh | | | |
| 047E2Fh | | | |
| 047E30h | | | |
| 047E31h | | | |
| 047E32h | | | |
| 047E33h | | | |
| 047E34h | | | |
| 047E35h | | | |
| 047E36h | | | |
| 047E37h | | | |
| 047E38h | | | |
| 047E39h | | | |
| 047E3Ah | | | |
| 047E3Bh | | | |
| 047E3Ch | | | |
| 047E3Dh | | | |
| 047E3Eh | | | |
| 047E3Fh | | | |
| 047E40h to 047F1Fh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.54 SFR List (54)

| Address | Register | Symbol | Reset Value |
|---------|----------------------------------|----------|-------------|
| 047F20h | CAN0 Message Control Register 0 | COMCTL0 | 00h |
| 047F21h | CAN0 Message Control Register 1 | COMCTL1 | 00h |
| 047F22h | CAN0 Message Control Register 2 | COMCTL2 | 00h |
| 047F23h | CAN0 Message Control Register 3 | COMCTL3 | 00h |
| 047F24h | CAN0 Message Control Register 4 | COMCTL4 | 00h |
| 047F25h | CAN0 Message Control Register 5 | COMCTL5 | 00h |
| 047F26h | CAN0 Message Control Register 6 | COMCTL6 | 00h |
| 047F27h | CAN0 Message Control Register 7 | COMCTL7 | 00h |
| 047F28h | CAN0 Message Control Register 8 | COMCTL8 | 00h |
| 047F29h | CAN0 Message Control Register 9 | COMCTL9 | 00h |
| 047F2Ah | CAN0 Message Control Register 10 | COMCTL10 | 00h |
| 047F2Bh | CAN0 Message Control Register 11 | COMCTL11 | 00h |
| 047F2Ch | CAN0 Message Control Register 12 | COMCTL12 | 00h |
| 047F2Dh | CAN0 Message Control Register 13 | COMCTL13 | 00h |
| 047F2Eh | CAN0 Message Control Register 14 | COMCTL14 | 00h |
| 047F2Fh | CAN0 Message Control Register 15 | COMCTL15 | 00h |
| 047F30h | CAN0 Message Control Register 16 | COMCTL16 | 00h |
| 047F31h | CAN0 Message Control Register 17 | COMCTL17 | 00h |
| 047F32h | CAN0 Message Control Register 18 | COMCTL18 | 00h |
| 047F33h | CAN0 Message Control Register 19 | COMCTL19 | 00h |
| 047F34h | CAN0 Message Control Register 20 | COMCTL20 | 00h |
| 047F35h | CAN0 Message Control Register 21 | COMCTL21 | 00h |
| 047F36h | CAN0 Message Control Register 22 | COMCTL22 | 00h |
| 047F37h | CAN0 Message Control Register 23 | COMCTL23 | 00h |
| 047F38h | CAN0 Message Control Register 24 | COMCTL24 | 00h |
| 047F39h | CAN0 Message Control Register 25 | COMCTL25 | 00h |
| 047F3Ah | CAN0 Message Control Register 26 | COMCTL26 | 00h |
| 047F3Bh | CAN0 Message Control Register 27 | COMCTL27 | 00h |
| 047F3Ch | CAN0 Message Control Register 28 | COMCTL28 | 00h |
| 047F3Dh | CAN0 Message Control Register 29 | COMCTL29 | 00h |
| 047F3Eh | CAN0 Message Control Register 30 | COMCTL30 | 00h |
| 047F3Fh | CAN0 Message Control Register 31 | COMCTL31 | 00h |

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.55 SFR List (55)

| Address | Register | Symbol | Reset Value |
|-----------------------|---|---------|-------------|
| 047F40h | CAN0 Control Register | C0CTLR | 0000 0101b |
| 047F41h | | | 0000 0000b |
| 047F42h | CAN0 Status Register | C0STR | 0000 0101b |
| 047F43h | | | 0000 0000b |
| 047F44h | CAN0 Bit Configuration Register | C0BCR | 00 0000h |
| 047F45h | | | |
| 047F46h | | | |
| 047F47h | CAN0 Clock Select Register | C0CLKR | 000X 0000b |
| 047F48h | CAN0 Receive FIFO Control Register | C0RFCR | 1000 0000b |
| 047F49h | CAN0 Receive FIFO Pointer Control Register | C0RFPCR | XXh |
| 047F4Ah | CAN0 Transmit FIFO Control Register | C0TFCR | 1000 0000b |
| 047F4Bh | CAN0 Transmit FIFO Pointer Control Register | C0TFPCR | XXh |
| 047F4Ch | CAN0 Error Interrupt Enable Register | C0EIER | 00h |
| 047F4Dh | CAN0 Error Interrupt Factor Judge Register | C0EIFR | 00h |
| 047F4Eh | CAN0 Receive Error Count Register | C0RECR | 00h |
| 047F4Fh | CAN0 Transmit Error Count Register | C0TECR | 00h |
| 047F50h | CAN0 Error Code Store Register | C0ECSR | 00h |
| 047F51h | CAN0 Channel Search Support Register | C0CSSR | XXh |
| 047F52h | CAN0 Mailbox Search Status Register | C0MSSR | 1000 0000b |
| 047F53h | CAN0 Mailbox Search Mode Register | C0MSMR | XXXX XX00b |
| 047F54h | CAN0 Time Stamp Register | C0TSR | 0000h |
| 047F55h | | | |
| 047F56h | CAN0 Acceptance Filter Support Register | C0AFSR | XXXXh |
| 047F57h | | | |
| 047F58h | CAN0 Test Control Register | C0TCR | 00h |
| 047F59h | | | |
| 047F5Ah | | | |
| 047F5Bh | | | |
| 047F5Ch | | | |
| 047F5Dh | | | |
| 047F5Eh | | | |
| 047F5Fh | | | |
| 047F60h to 047FFFh | | | |
| 048000h to 04FFFFh | | | |

X: Undefined

Blanks are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings (1)

| Symbol | Characteristic | | Condition | Value | Unit |
|-----------|-----------------------------|--|--------------------------|------------------------|------------------|
| V_{CC} | Supply voltage | | $V_{CC} = AV_{CC}$ | -0.3 to 6.0 | V |
| AV_{CC} | Analog supply voltage | | $V_{CC} = AV_{CC}$ | -0.3 to 6.0 | V |
| V_I | Input voltage | XIN, \overline{RESET} , CNVSS, NSD, V_{REF} , P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P17_4 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (2) | | -0.3 to $V_{CC} + 0.3$ | V |
| | | P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_3, P12_0 to P12_7, P16_0 to P16_7, P17_0 to P17_3 (2) | | -0.3 to 6.0 | V |
| V_O | Output voltage | XOUT, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (2) | | -0.3 to $V_{CC} + 0.3$ | V |
| P_d | Power consumption | | $T_a = 25^\circ\text{C}$ | 500 | mW |
| — | Operating temperature range | | | -40 to 85 | $^\circ\text{C}$ |
| T_{stg} | Storage temperature range | | | -65 to 150 | $^\circ\text{C}$ |

Notes:

- Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Ports P16 to P19 are available in the 176-pin package only.

Table 5.2 Operating Conditions (1/5) (1)

| Symbol | Characteristic | | Value | | | Unit | |
|----------------------|--|--|---|-----------------------|------------------------|-----------------|---|
| | | | Min. | Typ. | Max. | | |
| V _{CC} | Digital supply voltage | | 3.0 | 5.0 | 5.5 | V | |
| AV _{CC} | Analog supply voltage | | | V _{CC} | | V | |
| V _{REF} | Reference voltage | | 3.0 | | V _{CC} | V | |
| V _{SS} | Digital ground voltage | | | 0 | | V | |
| AV _{SS} | Analog ground voltage | | | 0 | | V | |
| dV _{CC} /dt | V _{CC} ramp up rate (V _{CC} < 2.0 V) | | 0.05 | | | V/ms | |
| V _{IH} | High level input voltage | XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P17_4 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3) | 0.8 × V _{CC} | | V _{CC} | V | |
| | | P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_3, P16_0 to P16_7, P17_0 to P17_3 (3) | 0.8 × V _{CC} | | 6.0 | V | |
| | | P0_0 to P0_7, P1_0 to P1_7, P13_0 to P13_7 | in single-chip mode | 0.8 × V _{CC} | | V _{CC} | V |
| | | | in memory expansion mode or microprocessor mode | 0.5 × V _{CC} | | V _{CC} | V |
| | | P12_0 to P12_7 | in single-chip mode | 0.8 × V _{CC} | | 6.0 | V |
| | | in memory expansion mode or microprocessor mode | 0.5 × V _{CC} | | 6.0 | V | |
| V _{IL} | Low level input voltage | XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3) | 0 | | 0.2 × V _{CC} | V | |
| | | P0_0 to P0_7, P1_0 to P1_7, P12_0 to P12_7, P13_0 to P13_7 | in single-chip mode | 0 | 0.2 × V _{CC} | V | |
| | | | in memory expansion mode or microprocessor mode | 0 | 0.16 × V _{CC} | V | |
| | | | | | | | |
| T _{opr} | Operating temperature range | N version | -20 | | 85 | °C | |
| | | D version | -40 | | 85 | °C | |
| | | P version | -40 | | 85 | °C | |

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. V_{IH} and V_{IL} for P8_7 are specified for P8_7 as a programmable port. These values are not applicable to P8_7 as XCIN.
3. Ports P16 to P19 are available in the 176-pin package only.

Table 5.3 Operating Conditions (2/5)
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) (1)

| Symbol | Characteristic | | Value (2) | | | Unit |
|-----------|--|--------------------------|-----------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| C_{VDC} | Decoupling capacitance for voltage regulator | Inter-pin voltage: 1.5 V | 2.4 | | 10.0 | μ F |

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. This value should be satisfied with due consideration of every condition as follows: operating temperature, DC bias, aging, etc.

Table 5.4 Operating Conditions (3/5)
 ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) (1)

| Symbol | Characteristic | Value | | | Unit |
|----------------|---|-------|------|-------|------|
| | | Min. | Typ. | Max. | |
| $I_{OH(peak)}$ | High level peak output current (2) P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3) | | | -10.0 | mA |
| $I_{OH(avg)}$ | High level average output current (4) P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3) | | | -5.0 | mA |
| $I_{OL(peak)}$ | Low level peak output current (2) P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3) | | | 10.0 | mA |
| $I_{OL(avg)}$ | Low level average output current (4) P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3) | | | 5.0 | mA |

Notes:

- The device is operationally guaranteed under these operating conditions.
- The following conditions should be satisfied:
 - The sum of $I_{OL(peak)}$ of ports P0, P1, P2, P8_6, P8_7, P9, P10, P11_0 to P11_4, P14_3 to P14_6, P15, P18_2 to P18_7, P19_0, P19_1, P19_6, and P19_7 is 80 mA or less.
 - The sum of $I_{OL(peak)}$ of ports P3, P4, P5, P6, P7, P8_0 to P8_4, P11_5 to P11_7, P12, P13, P14_7, P16, P17, P18_0, P18_1, and P19_2 to P19_5 is 80 mA or less.
 - The sum of $I_{OH(peak)}$ of ports P0, P1, P2, P11_0 to P11_4, P18_2 to P18_7, P19_0, and P19_1 is -40 mA or less.
 - The sum of $I_{OH(peak)}$ of ports P8_6, P8_7, P9, P10, P14_3 to P14_6, P15, P19_6, and P19_7 is -40 mA or less.
 - The sum of $I_{OH(peak)}$ of ports P3, P4, P5, P11_5, P11_6, P12, P13, P16, P17_0 to P17_3, and P19_2 to P19_5 is -40 mA or less.
 - The sum of $I_{OH(peak)}$ of ports P6, P7, P8_0 to P8_4, P11_7, P14_7, P17_4 to P17_7, P18_0, and P18_1 is -40 mA or less.
- Ports P16 to P19 are available in the 176-pin package only.
- Average value within 100 ms.

Table 5.5 Operating Conditions (4/5)
 ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) (1)

| Symbol | Characteristic | Value | | | Unit |
|---------------|--|--------|--------|------|------|
| | | Min. | Typ. | Max. | |
| $f_{(XIN)}$ | Main clock oscillator frequency | 4 | | 16 | MHz |
| $f_{(XRef)}$ | Reference clock frequency | 2 | | 4 | MHz |
| $f_{(PLL)}$ | PLL clock oscillator frequency | 96 | | 128 | MHz |
| $f_{(Base)}$ | Base clock frequency | | | 64 | MHz |
| $t_{c(Base)}$ | Base clock cycle time | 15.625 | | | ns |
| $f_{(CPU)}$ | CPU operating frequency | | | 64 | MHz |
| $t_{c(CPU)}$ | CPU clock cycle time | 15.625 | | | ns |
| $f_{(BCLK)}$ | Peripheral bus clock operating frequency | | | 32 | MHz |
| $t_{c(BCLK)}$ | Peripheral bus clock cycle time | 31.25 | | | ns |
| $f_{(PER)}$ | Peripheral clock source frequency | | | 32 | MHz |
| $f_{(XCIN)}$ | Sub clock oscillator frequency | | 32.768 | 62.5 | kHz |

Note:

1. The device is operationally guaranteed under these operating conditions.

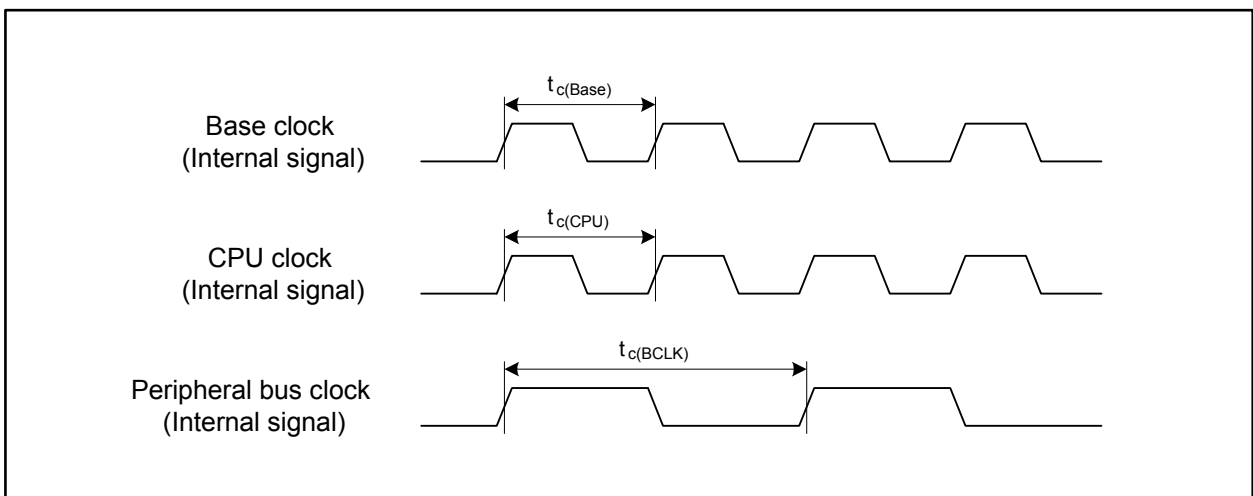


Figure 5.1 Clock Cycle Time

Table 5.6 Operating Conditions (5/5)
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) (1)

| Symbol | Characteristic | Value | | | Unit |
|------------------|----------------------------|------------------|------|-----------|------|
| | | Min. | Typ. | Max. | |
| $V_{r(VCC)}$ | Allowable ripple voltage | $V_{CC} = 5.0$ V | | 0.5 | Vp-p |
| | | $V_{CC} = 3.0$ V | | 0.3 | Vp-p |
| $dV_{r(VCC)}/dt$ | Ripple voltage gradient | $V_{CC} = 5.0$ V | | ± 0.3 | V/ms |
| | | $V_{CC} = 3.0$ V | | ± 0.3 | V/ms |
| $f_{r(VCC)}$ | Allowable ripple frequency | | | 10 | kHz |

Note:

- The device is operationally guaranteed under these operating conditions.

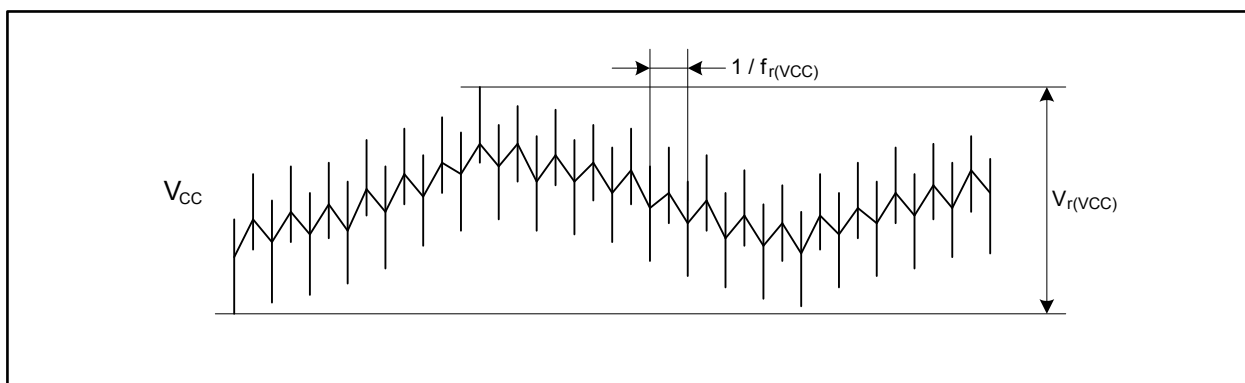


Figure 5.2 Ripple Waveform

Table 5.7 RAM Electrical Characteristics
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit |
|-----------|----------------------------|-----------------------|-------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V_{RDR} | RAM data retention voltage | in stop mode | 2.0 | | | V |

Table 5.8 Flash Memory Electrical Characteristics
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristic | | Value | | | Unit |
|------------|---|------------------------------|-------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| — | Programming and erasure endurance of flash memory (1) | Program area | 1000 | | | times |
| | | Data area | 10000 | | | times |
| — | 4-word program time | Program area | | 150 | 900 | μ s |
| | | Data area | | 300 | 1700 | μ s |
| — | Lock bit-program time | Program area | | 70 | 500 | μ s |
| | | Data area | | 140 | 1000 | μ s |
| — | Block erasure time | 4 Kbyte block | | 0.12 | 3.0 | s |
| | | 32 Kbyte block | | 0.17 | 3.0 | s |
| | | 64 Kbyte block | | 0.20 | 3.0 | s |
| t_{SUSP} | Suspend latency | | | | 250 | μ s |
| — | Data retention (2) | $T_a = 55^\circ\text{C}$ (3) | 10 | | | years |

Notes:

1. Program/erase definition

This value represents the number of erasures per block.

If the flash memory is programmed/erased n times, each block can be erased n times.

i.e. If 4-word write is performed in 512 different addresses in the block A of 4 Kbyte and then the block is erased, it is considered the programming/erasure is performed just once.

However a write in the same address more than once for one erasure is disabled (overwrite disabled).

2. The data retention time includes the periods when the supply voltage is not applied and no clock is provided.

3. Please contact a Renesas Electronics sales office regarding data retention time other than the above.

Table 5.9 Power Supply Circuit Timing Characteristics
 ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit |
|--------------|--|-----------------------|-------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Internal power supply start-up stabilization time after the main power supply is turned on | | | | 2 | ms |

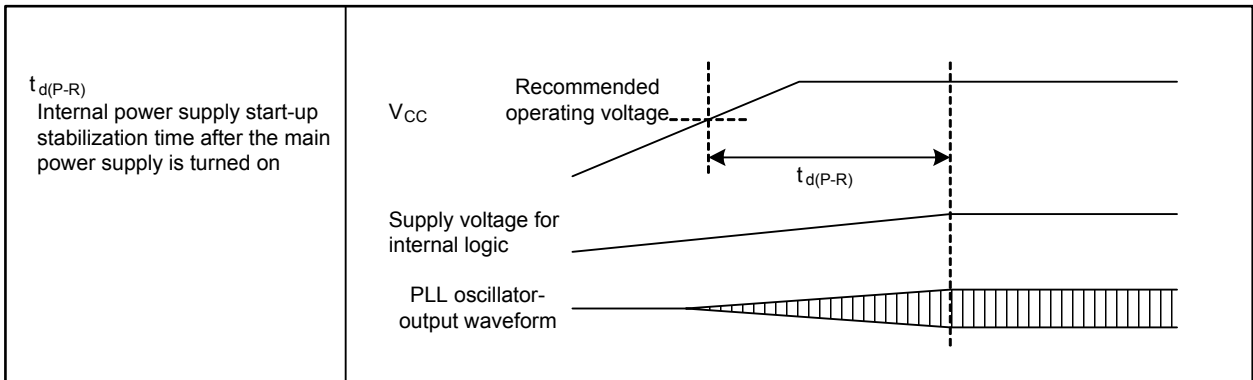


Figure 5.3 Power Supply Circuit Timing

Table 5.10 Electrical Characteristics of Voltage Regulator for Internal Logic
 ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristics | Measurement condition | Value | | | Unit |
|------------|-----------------|-----------------------|-------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V_{VDC1} | Output voltage | | | 1.5 | | V |

Table 5.11 Electrical Characteristics of Low Voltage Detector
 ($V_{CC} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristics | Measurement condition | Value | | | Unit |
|---------------------------|--|--|-------|------|-----------|---------|
| | | | Min. | Typ. | Max. | |
| ΔV_{det} | Detected voltage error | | | | ± 0.3 | V |
| $V_{det(R)} - V_{det(F)}$ | Hysteresis width | | 0 | | | V |
| — | Self-consuming current | $V_{CC} = 5.0$ V, low voltage detector enabled | | 4 | | μA |
| $t_{d(E-A)}$ | Operation start time of low voltage detector | | | | 150 | μs |

Table 5.12 Electrical Characteristics of Oscillator
 ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristics | Measurement condition | Value | | | Unit |
|-------------------|--------------------------------------|-----------------------|-------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $f_{SO(PLL)}$ | PLL clock self-oscillation frequency | | 35 | 55 | 80 | MHz |
| $t_{LOCK(PLL)}$ | PLL lock time (1) | | | | 1 | ms |
| $t_{jitter(p-p)}$ | PLL jitter period (p-p) | | | | 2.0 | ns |
| $f_{(OCO)}$ | On-chip oscillator frequency | | 62.5 | 125 | 250 | kHz |

Note:

1. This value is applicable only when the main clock oscillation is stable.

Table 5.13 Electrical Characteristics of Clock Circuitry
 ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristics | Measurement condition | Value | | | Unit |
|-----------------|--|-----------------------|-------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| $t_{rec(WAIT)}$ | Recovery time from wait mode to low power mode | | | | 225 | μ s |
| $t_{rec(STOP)}$ | Recovery time from stop mode (1) | | | | 225 | μ s |

Note:

1. This recovery time does not include the period until the main clock oscillator is stabilized. The CPU starts operating before the oscillator is stabilized.

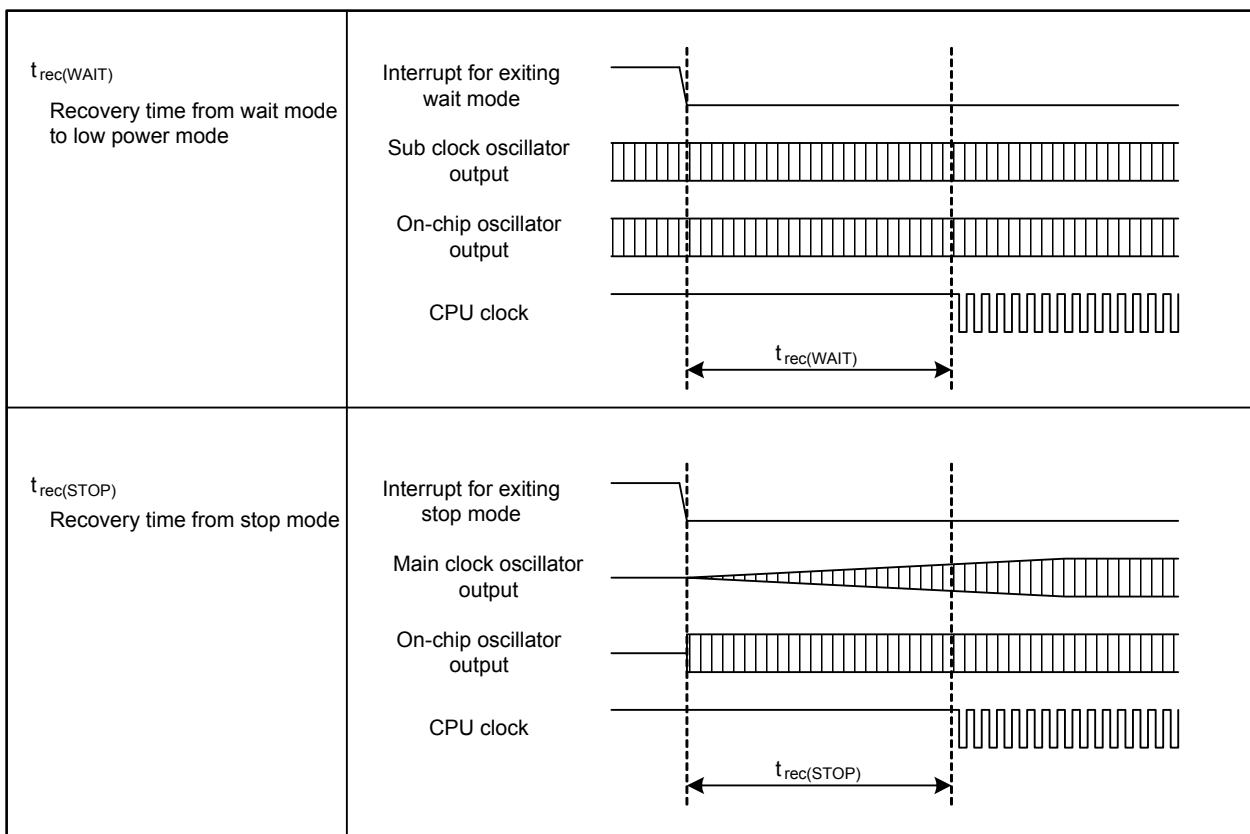


Figure 5.4 Clock Circuit Timing

Timing Requirements ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.14 Flash Memory CPU Rewrite Mode Timing

| Symbol | Characteristics | Value | | Unit |
|---------------|-----------------------------------|-------|------|------|
| | | Min. | Max. | |
| t_{cR} | Read cycle time | 200 | | ns |
| $t_{su(S-R)}$ | Chip-select setup time for read | 200 | | ns |
| $t_{h(R-S)}$ | Chip-select hold time after read | 0 | | ns |
| $t_{su(A-R)}$ | Address setup time for read | 200 | | ns |
| $t_{h(R-A)}$ | Address hold time after read | 0 | | ns |
| $t_{w(R)}$ | Read pulse width | 100 | | ns |
| t_{cW} | Write cycle time | 200 | | ns |
| $t_{su(S-W)}$ | Chip-select setup time for write | 0 | | ns |
| $t_{h(W-S)}$ | Chip-select hold time after write | 30 | | ns |
| $t_{su(A-W)}$ | Address setup time for write | 0 | | ns |
| $t_{h(W-A)}$ | Address hold time after write | 30 | | ns |
| $t_{w(W)}$ | Write pulse width | 50 | | ns |

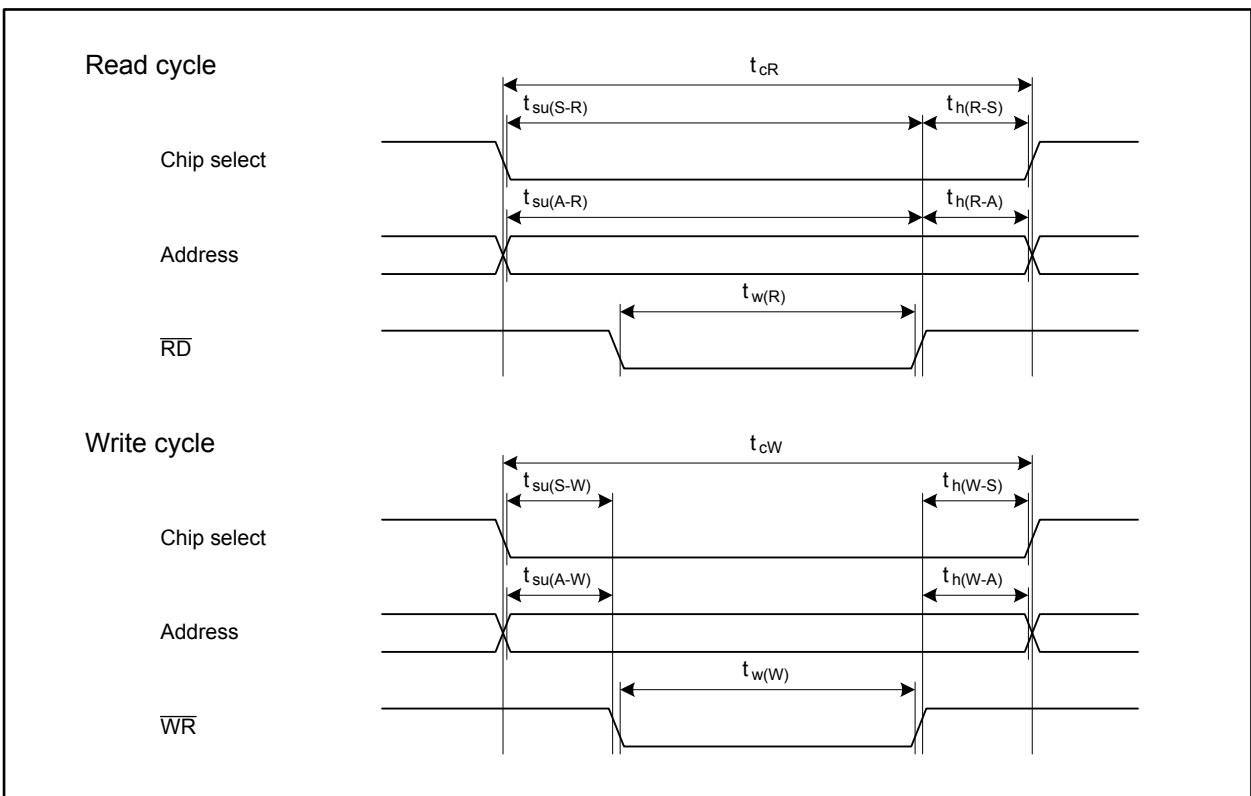


Figure 5.5 Flash Memory CPU Rewrite Mode Timing

$$V_{CC} = 5 \text{ V}$$

Table 5.15 Electrical Characteristics (1/3)

($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(CPU)} = 64 \text{ MHz}$, unless otherwise noted)

| Symbol | Characteristic | | Measurement condition | Value | | | Unit |
|----------|---------------------------|--|-----------------------------|----------------|------|----------|------|
| | | | | Min. | Typ. | Max. | |
| V_{OH} | High level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $I_{OH} = -5 \text{ mA}$ | $V_{CC} - 2.0$ | | V_{CC} | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $I_{OH} = -200 \mu\text{A}$ | $V_{CC} - 0.3$ | | V_{CC} | V |
| V_{OL} | Low level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $I_{OL} = 5 \text{ mA}$ | | | 2.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $I_{OL} = 200 \mu\text{A}$ | | | 0.45 | V |

Note:

1. Ports P16 to P19 are available in the 176-pin package only.

$V_{CC} = 5\text{ V}$

Table 5.16 Electrical Characteristics (2/3) $(V_{CC} = 4.2\text{ to }5.5\text{ V}, V_{SS} = 0\text{ V}, T_a = T_{opr}, \text{ and } f_{(CPU)} = 64\text{ MHz, unless otherwise noted})$

| Symbol | Characteristic | Measurement condition | Value | | | Unit | |
|-------------------|--------------------------|---|--------------------|------|------|------------------|------------------|
| | | | Min. | Typ. | Max. | | |
| $V_{T+} - V_{T-}$ | Hysteresis | HOLD, RDY, NMI, INT0 to INT8, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS10, CLK0 to CLK10, RXD0 to RXD10, SCL0 to SCL6, SDA0 to SDA6, SS0 to SS6, SRXD0 to SRXD6, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN, CAN0IN, CAN1IN, CAN0WU, CAN1WU | | 0.2 | 1.0 | V | |
| | | RESET | | 0.2 | 1.8 | V | |
| I_{IH} | High level input current | XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $V_I = 5\text{ V}$ | | 5.0 | μA | |
| I_{IL} | Low level input current | XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $V_I = 0\text{ V}$ | | -5.0 | μA | |
| R_{PULLUP} | Pull-up resistor | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P17_4 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $V_I = 0\text{ V}$ | 30 | 50 | 170 | $\text{k}\Omega$ |
| R_{fXIN} | Feedback resistor | XIN | | 1.5 | | $\text{M}\Omega$ | |
| R_{fXCIN} | Feedback resistor | XCIN | | 15 | | $\text{M}\Omega$ | |

Note:

- Ports P16 to P19 are available in the 176-pin package only.

$$V_{CC} = 5 V$$

Table 5.17 Electrical Characteristics (3/3)
($V_{CC} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit | | |
|----------|----------------------|---|---|--|------|------|------|---------|
| | | | Min. | Typ. | Max. | | | |
| I_{CC} | Power supply current | In single-chip mode, output pins are left open and others are connected to V_{SS} | $f_{(CPU)} = 64$ MHz, $f_{(BCLK)} = 32$ MHz, $f_{(XIN)} = 8$ MHz, Active: XIN, PLL, Stopped: XCIN, OCO | | 45 | 60 | mA | |
| | | | XIN-XOUT Drive power: | $f_{(CPU)} = f_{SO(PLL)}/24$ MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO | | 12 | | mA |
| | | | XCIN-XCOUT Drive power: low | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256$ MHz, $f_{(XIN)} = 8$ MHz, Active: XIN, Stopped: PLL, XCIN, OCO | | 1.2 | | mA |
| | | | | $f_{(CPU)} = f_{(BCLK)} = 32.768$ kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown | | 220 | | μ A |
| | | | | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4$ kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown | | 230 | | μ A |
| | | | | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256$ MHz, $f_{(XIN)} = 8$ MHz, Active: XIN, Stopped: PLL, XCIN, OCO, $T_a = 25^\circ\text{C}$, Wait mode | | 960 | 1600 | μ A |
| | | | | $f_{(CPU)} = f_{(BCLK)} = 32.768$ kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, $T_a = 25^\circ\text{C}$, Wait mode | | 8 | 140 | μ A |
| | | | | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4$ kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, $T_a = 25^\circ\text{C}$, Wait mode | | 10 | 150 | μ A |
| | | | | Stopped: all clocks, Main regulator: shutdown, $T_a = 25^\circ\text{C}$ | | 5 | 70 | μ A |

$$V_{CC} = 5 \text{ V}$$

Table 5.18 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 4.2$ to 5.5 V , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(BCLK)} = 32 \text{ MHz}$, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit |
|---------------|---|--|---------------------------------|---------|-----------|---------------|
| | | | Min. | Typ. | Max. | |
| — | Resolution | $V_{REF} = V_{CC}$ | | | 10 | Bits |
| — | Absolute error | $V_{REF} = V_{CC} = 5 \text{ V}$ AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 | | | ± 3 | LSB |
| | | | External op-amp connection mode | | ± 7 | LSB |
| INL | Integral non-linearity error | $V_{REF} = V_{CC} = 5 \text{ V}$ AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 | | | ± 3 | LSB |
| | | | External op-amp connection mode | | ± 7 | LSB |
| DNL | Differential non-linearity error | | | ± 1 | LSB | |
| — | Offset error | | | ± 3 | LSB | |
| — | Gain error | | | ± 3 | LSB | |
| R_{LADDER} | Resistor ladder | $V_{REF} = V_{CC}$ | 4 | | 20 | $k\Omega$ |
| t_{CONV} | Conversion time (10 bits) | $\phi_{AD} = 16 \text{ MHz}$, with sample and hold function | 2.06 | | | μs |
| | | $\phi_{AD} = 16 \text{ MHz}$, without sample and hold function | 3.69 | | | μs |
| t_{CONV} | Conversion time (8 bits) | $\phi_{AD} = 16 \text{ MHz}$, with sample and hold function | 1.75 | | | μs |
| | | $\phi_{AD} = 16 \text{ MHz}$, without sample and hold function | 3.06 | | | μs |
| t_{SAMP} | Sampling time | $\phi_{AD} = 16 \text{ MHz}$ | 0.188 | | | μs |
| V_{IA} | Analog input voltage | | 0 | | V_{REF} | V |
| ϕ_{AD} | Operating clock frequency | without sample and hold function | 0.25 | | 16 | MHz |
| | | with sample and hold function | 1 | | 16 | MHz |
| $R_{PU(AST)}$ | Pull-up resistor for open-circuit detection | | 5 | 10 | 15 | $k\Omega$ |
| $R_{PD(AST)}$ | Pull-down resistor for open-circuit detection | | 5 | 10 | 15 | $k\Omega$ |

$$V_{CC} = 5 \text{ V}$$

Table 5.19 D/A Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 4.2$ to 5.5 V , $V_{SS} = AV_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit |
|------------|-------------------------|-----------------------|-------|------|------|------------------|
| | | | Min. | Typ. | Max. | |
| — | Resolution | | | | 8 | Bits |
| — | Absolute precision | | | | 1.0 | % |
| t_s | Settling time | | | | 3 | μs |
| R_O | Output resistance | | 4 | 10 | 20 | $\text{k}\Omega$ |
| I_{VREF} | Reference input current | (1) | | | 1.5 | mA |

Note:

- One D/A converter is used. The DAi register ($i = 0, 1$) of the other unused converter is set to 00h. The resistor ladder for A/D converter is not considered.
Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

$$V_{CC} = 5 \text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.20 External Clock Input

| Symbol | Characteristic | Value | | Unit |
|-------------|---|-------|------|------|
| | | Min. | Max. | |
| $t_{C(X)}$ | External clock input period | 62.5 | 250 | ns |
| $t_{W(XH)}$ | External clock input high level pulse width | 25 | | ns |
| $t_{W(XL)}$ | External clock input low level pulse width | 25 | | ns |
| $t_{r(X)}$ | External clock input rise time | | 5 | ns |
| $t_{f(X)}$ | External clock input fall time | | 5 | ns |
| t_W / t_C | External clock input duty | 40 | 60 | % |

Table 5.21 External Bus Timing

| Symbol | Characteristic | Value | | Unit |
|----------------|------------------------------|-------|-------------------------------|------|
| | | Min. | Max. | |
| $t_{su(D-R)}$ | Data setup time for read | 40 | | ns |
| $t_h(R-D)$ | Data hold time after read | 0 | | ns |
| $t_{dis(R-D)}$ | Data disable time after read | | $0.5 \times t_{C(Base)} + 10$ | ns |

$$V_{CC} = 5 \text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.22 Timer A Input (Counting input in event counter mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{C(TA)}$ | TAiIN input clock cycle time | 200 | | ns |
| $t_{W(TAH)}$ | TAiIN input high level pulse width | 80 | | ns |
| $t_{W(TAL)}$ | TAiIN input low level pulse width | 80 | | ns |

Table 5.23 Timer A Input (Gating input in timer mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{C(TA)}$ | TAiIN input clock cycle time | 400 | | ns |
| $t_{W(TAH)}$ | TAiIN input high level pulse width | 180 | | ns |
| $t_{W(TAL)}$ | TAiIN input low level pulse width | 180 | | ns |

Table 5.24 Timer A Input (External trigger input in one-shot timer mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{C(TA)}$ | TAiIN input clock cycle time | 200 | | ns |
| $t_{W(TAH)}$ | TAiIN input high level pulse width | 80 | | ns |
| $t_{W(TAL)}$ | TAiIN input low level pulse width | 80 | | ns |

Table 5.25 Timer A Input (External trigger input in pulse-width modulation mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{W(TAH)}$ | TAiIN input high level pulse width | 80 | | ns |
| $t_{W(TAL)}$ | TAiIN input low level pulse width | 80 | | ns |

Table 5.26 Timer A Input (Increment/decrement count switching input in event counter mode)

| Symbol | Characteristic | Value | | Unit |
|------------------|-------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{C(UP)}$ | TAiOUT input clock cycle time | 2000 | | ns |
| $t_{W(UPH)}$ | TAiOUT input high level pulse width | 1000 | | ns |
| $t_{W(UPL)}$ | TAiOUT input low level pulse width | 1000 | | ns |
| $t_{Su(UP-TIN)}$ | TAiOUT input setup time | 400 | | ns |
| $t_h(TIN-UP)$ | TAiOUT input hold time | 400 | | ns |

$$V_{CC} = 5 \text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.27 Timer B Input (Counting input in event counter mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|--|-------|------|------|
| | | Min. | Max. | |
| $t_{C(TB)}$ | TBiIN input clock cycle time (one edge counting) | 200 | | ns |
| $t_{W(TBH)}$ | TBiIN input high level pulse width (one edge counting) | 80 | | ns |
| $t_{W(TBL)}$ | TBiIN input low level pulse width (one edge counting) | 80 | | ns |
| $t_{C(TB)}$ | TBiIN input clock cycle time (both edges counting) | 200 | | ns |
| $t_{W(TBH)}$ | TBiIN input high level pulse width (both edges counting) | 80 | | ns |
| $t_{W(TBL)}$ | TBiIN input low level pulse width (both edges counting) | 80 | | ns |

Table 5.28 Timer B Input (Pulse period measure mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{C(TB)}$ | TBiIN input clock cycle time | 400 | | ns |
| $t_{W(TBH)}$ | TBiIN input high level pulse width | 180 | | ns |
| $t_{W(TBL)}$ | TBiIN input low level pulse width | 180 | | ns |

Table 5.29 Timer B Input (Pulse-width measure mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{C(TB)}$ | TBiIN input clock cycle time | 400 | | ns |
| $t_{W(TBH)}$ | TBiIN input high level pulse width | 180 | | ns |
| $t_{W(TBL)}$ | TBiIN input low level pulse width | 180 | | ns |

$$V_{CC} = 5 \text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.30 Serial Interface

| Symbol | Characteristic | Value | | Unit |
|---------------|-----------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input clock cycle time | 200 | | ns |
| $t_{W(CKH)}$ | CLKi input high level pulse width | 80 | | ns |
| $t_{W(CKL)}$ | CLKi input low level pulse width | 80 | | ns |
| $t_{su(D-C)}$ | RXD _i input setup time | 80 | | ns |
| $t_{h(C-D)}$ | RXD _i input hold time | 90 | | ns |

Table 5.31 A/D Trigger Input

| Symbol | Characteristic | Value | | Unit |
|--------------|---|-----------------------|------|------|
| | | Min. | Max. | |
| $t_{W(ADH)}$ | ADTRG input high level pulse width Hardware trigger input high level pulse width | $\frac{3}{\phi_{AD}}$ | | ns |
| $t_{W(ADL)}$ | ADTRG input low level pulse width Hardware trigger input high level pulse width | 125 | | ns |

Table 5.32 External Interrupt INT_i Input

| Symbol | Characteristic | | Value | | Unit |
|--------------|---|-----------------|--------------------|------|------|
| | | | Min. | Max. | |
| $t_{W(INH)}$ | INT _i input high level pulse width | Edge sensitive | 250 | | ns |
| | | Level sensitive | $t_{C(CPU)} + 200$ | | ns |
| $t_{W(INL)}$ | INT _i input low level pulse width | Edge sensitive | 250 | | ns |
| | | Level sensitive | $t_{C(CPU)} + 200$ | | ns |

Table 5.33 Intelligent I/O

| Symbol | Characteristic | Value | | Unit |
|----------------------|-------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(ISCLK2)}$ | ISCLK2 input clock cycle time | 600 | | ns |
| $t_{W(ISCLK2H)}$ | ISCLK2 input high level pulse width | 270 | | ns |
| $t_{W(ISCLK2L)}$ | ISCLK2 input low level pulse width | 270 | | ns |
| $t_{su(RXD-ISCLK2)}$ | ISRXD2 input setup time | 150 | | ns |
| $t_{h(ISCLK2-RXD)}$ | ISRXD2 input hold time | 100 | | ns |

$$V_{CC} = 5 \text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.34 Multi-master I²C-bus Interface

| Symbol | Characteristic | Value | | | | Unit |
|--------------------|---|---------------|------|---------------------------------|------|------|
| | | Standard-mode | | Fast-mode | | |
| | | Min. | Max. | Min. | Max. | |
| $t_{w(SCLH)}$ | MSCL input high level pulse width | 600 | | 600 | | ns |
| $t_{w(SCLL)}$ | MSCL input low level pulse width | 600 | | 600 | | ns |
| $t_{r(SCL)}$ | MSCL input rise time | | 1000 | | 300 | ns |
| $t_{f(SCL)}$ | MSCL input fall time | | 300 | | 300 | ns |
| $t_{r(SDA)}$ | MSDA input rise time | | 1000 | | 300 | ns |
| $t_{f(SDA)}$ | MSDA input fall time | | 300 | | 300 | ns |
| $t_{h(SDA-SCL)S}$ | MSCL high level hold time after start condition/restart condition | (1) | | $2 \times t_{c(\phi IIC)} + 40$ | | ns |
| $t_{su(SCL-SDA)P}$ | MSCL high level setup time for restart condition/stop condition | (1) | | $2 \times t_{c(\phi IIC)} + 40$ | | ns |
| $t_{w(SDAH)P}$ | MSDA high level pulse width after stop condition | (1) | | $4 \times t_{c(\phi IIC)} + 40$ | | ns |
| $t_{su(SDA-SCL)}$ | MSDA input setup time | 100 | | 100 | | ns |
| $t_{h(SCL-SDA)}$ | MSDA input hold time | 0 | | 0 | | ns |

Note:

- The value is calculated by the following formulas based on a value SSC set by bits SSC4 to SSC0 in the I2CSSCR register:

$$t_{h(SDA-SCL)S} = SSC \div 2 \times t_{c(\phi IIC)} + 40 \text{ [ns]}$$

$$t_{su(SCL-SDA)P} = (SSC \div 2 + 1) \times t_{c(\phi IIC)} + 40 \text{ [ns]}$$

$$t_{w(SDAH)P} = (SSC + 1) \times t_{c(\phi IIC)} + 40 \text{ [ns]}$$

$$V_{CC} = 5 \text{ V}$$

Switching Characteristics ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.35 External Bus Timing (Separate bus)

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|---------------|-----------------------------------|-----------------------|-------------------------------|------|------|
| | | | Min. | Max. | |
| $t_{su(S-R)}$ | Chip-select setup time for read | Refer to Figure 5.6 | (1) | | ns |
| $t_{h(R-S)}$ | Chip-select hold time after read | | $t_{c(Base)} - 15$ | | ns |
| $t_{su(A-R)}$ | Address setup time for read | | (1) | | ns |
| $t_{h(R-A)}$ | Address hold time after read | | $t_{c(Base)} - 15$ | | ns |
| $t_{w(R)}$ | Read pulse width | | (1) | | ns |
| $t_{su(S-W)}$ | Chip-select setup time for write | | (1) | | ns |
| $t_{h(W-S)}$ | Chip-select hold time after write | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{su(A-W)}$ | Address setup time for write | | (1) | | ns |
| $t_{h(W-A)}$ | Address hold time after write | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{w(W)}$ | Write pulse width | | (1) | | ns |
| $t_{su(D-W)}$ | Data setup time for write | | (1) | | ns |
| $t_{h(W-D)}$ | Data hold time after write | | 0 | | ns |

Note:

- The value is calculated by the following formulas based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_{w(R)}$, $T_{su(A-W)}$, and $T_{w(W)}$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For the details of how to set values, refer to the User's manual.

$$t_{su(S-R)} = t_{su(A-R)} = T_{su(A-R)} \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(R)} = T_{w(R)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$t_{su(S-W)} = t_{su(A-W)} = T_{su(A-W)} \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(W)} = t_{su(D-W)} = T_{w(W)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$V_{CC} = 5 V$$

Switching Characteristics ($V_{CC} = 4.2$ to $5.5 V$, $V_{SS} = 0 V$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.36 External Bus Timing (Multiplexed bus)

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|-----------------|-----------------------------------|-----------------------|-------------------------------|------------------------|------|
| | | | Min. | Max. | |
| $t_{su(S-ALE)}$ | Chip-select setup time for ALE | Refer to Figure 5.6 | (1) | | ns |
| $t_{h(R-S)}$ | Chip-select hold time after read | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{su(A-ALE)}$ | Address setup time for ALE | | (1) | | ns |
| $t_{h(ALE-A)}$ | Address hold time after ALE | | $t_{c(Base)} - 5$ (2) | | ns |
| $t_{h(R-A)}$ | Address hold time after read | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{d(ALE-R)}$ | ALE-read delay time | | $t_{c(Base)} - 5$ (2) | $t_{c(Base)} + 10$ (2) | ns |
| $t_{w(ALE)}$ | ALE pulse width | | (1) | | ns |
| $t_{dis(R-A)}$ | Address disable time after read | | | 8 | ns |
| $t_{w(R)}$ | Read pulse width | | (1) | | ns |
| $t_{h(W-S)}$ | Chip-select hold time after write | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{h(W-A)}$ | Address hold time after write | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{d(ALE-W)}$ | ALE-write delay time | | $t_{c(Base)} - 5$ (2) | $t_{c(Base)} + 10$ (2) | ns |
| $t_{w(W)}$ | Write pulse width | | (1) | | ns |
| $t_{su(D-W)}$ | Data setup time for write | | (1) | | ns |
| $t_{h(W-D)}$ | Data hold time after write | | $0.5 \times t_{c(Base)}$ | | ns |

Notes:

- The value is calculated by the following formulas based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_w(R)$, $T_{su(A-W)}$, and $T_w(W)$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For the details of how to set values, refer to the User's manual.

$$t_{su(S-ALE)} = t_{su(A-ALE)} = t_{w(ALE)} = (T_{su(A-R)} - 1) \times t_{c(Base)} - 15 \text{ [ns]}$$
 (when $T_{su(A-R)}$ is greater than 1)

$$t_{su(S-ALE)} = t_{su(A-ALE)} = t_{w(ALE)} = 0.5 \times t_{c(Base)} - 15 \text{ [ns]}$$
 (when $T_{su(A-R)}$ is 1)

$$t_{w(R)} = T_w(R) \times t_{c(Base)} - 10 \text{ [ns]}$$

$$t_{w(W)} = t_{su(D-W)} = T_w(W) \times t_{c(Base)} - 10 \text{ [ns]}$$
- When $T_{su(A-R)}$ is greater than 1 or $T_{su(A-W)}$ is greater than 1. Change " $t_{c(Base)}$ " to " $0.5 \times t_{c(Base)}$ " when $T_{su(A-R)}$ is 1 or $T_{su(A-W)}$ is 1.

$$V_{CC} = 5 \text{ V}$$

Switching Characteristics ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.37 Serial Interface

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|--------------|------------------------|-----------------------|-------|------|------|
| | | | Min. | Max. | |
| $t_{d(C-Q)}$ | TXDi output delay time | Refer to Figure 5.6 | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi output hold time | | 0 | | ns |

Table 5.38 Intelligent I/O

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|-----------------|--------------------------|-----------------------|-------|------|------|
| | | | Min. | Max. | |
| $t_{d(ISTXD2)}$ | ISTXD2 output delay time | Refer to Figure 5.6 | | 180 | ns |
| $t_{h(ISTXD2)}$ | ISTXD2 output hold time | | 0 | | ns |

Table 5.39 Multi-master I²C-bus Interface (Standard-mode)

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|-------------------|--|-----------------------|-----------------------------------|-----------------------------------|------|
| | | | Min. | Max. | |
| $t_{f(SCL)}$ | MSCL output fall time | Refer to Figure 5.6 | 2 | | ns |
| $t_{f(SDA)}$ | MSDA output fall time | | 2 | | ns |
| $t_{d(SDA-SCL)S}$ | MSCL output delay time after start condition/restart condition | | $20 \times t_{c(\phi IIC)} - 120$ | $52 \times t_{c(\phi IIC)} - 40$ | ns |
| $t_{d(SCL-SDA)P}$ | Restart condition/stop condition output delay time after MSCL becomes high | | $20 \times t_{c(\phi IIC)} + 40$ | $52 \times t_{c(\phi IIC)} + 120$ | ns |
| $t_{d(SCL-SDA)}$ | MSDA output delay time | | $2 \times t_{c(\phi IIC)} + 40$ | $3 \times t_{c(\phi IIC)} + 120$ | ns |

Table 5.40 Multi-master I²C-bus Interface (Fast-mode)

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|-------------------|--|-----------------------|-----------------------------------|-----------------------------------|------|
| | | | Min. | Max. | |
| $t_{f(SCL)}$ | MSCL output fall time | Refer to Figure 5.6 | 2 (1) | | ns |
| $t_{f(SDA)}$ | MSDA output fall time | | 2 (1) | | ns |
| $t_{d(SDA-SCL)S}$ | MSCL output delay time after start condition/restart condition | | $10 \times t_{c(\phi IIC)} - 120$ | $26 \times t_{c(\phi IIC)} - 40$ | ns |
| $t_{d(SCL-SDA)P}$ | Restart condition/stop condition output delay time after MSCL becomes high | | $10 \times t_{c(\phi IIC)} + 40$ | $26 \times t_{c(\phi IIC)} + 120$ | ns |
| $t_{d(SCL-SDA)}$ | MSDA output delay time | | $2 \times t_{c(\phi IIC)} + 40$ | $3 \times t_{c(\phi IIC)} + 120$ | ns |

Note:

- External circuits are required to satisfy the I²C-bus specification.

$$V_{CC} = 3.3 \text{ V}$$

Table 5.41 Electrical Characteristics (1/3) ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(CPU)} = 64 \text{ MHz}$, unless otherwise noted)

| Symbol | Characteristic | | Measurement condition | Value | | | Unit |
|----------|---------------------------|--|--------------------------|----------------|------|----------|------|
| | | | | Min. | Typ. | Max. | |
| V_{OH} | High level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $I_{OH} = -1 \text{ mA}$ | $V_{CC} - 0.6$ | | V_{CC} | V |
| V_{OL} | Low level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $I_{OL} = 1 \text{ mA}$ | | | 0.5 | V |

Note:

1. Ports P16 to P19 are available in the 176-pin package only.

$$V_{CC} = 3.3 \text{ V}$$

Table 5.42 Electrical Characteristics (2/3) ($V_{CC} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 64$ MHz, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit | |
|-------------------|--------------------------|---|-----------------------|------|------|------------------|------------------|
| | | | Min. | Typ. | Max. | | |
| $V_{T+} - V_{T-}$ | Hysteresis | HOLD, RDY, NMI, INT0 to INT8, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS10, CLK0 to CLK10, RXD0 to RXD10, SCL0 to SCL6, SDA0 to SDA6, SS0 to SS6, SRXD0 to SRXD6, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN, CAN0IN, CAN1IN, CAN0WU, CAN1WU | | | | V | |
| | | RESET | 0.2 | | 1.8 | V | |
| I_{IH} | High level input current | XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $V_I = 3.3 \text{ V}$ | | 4.0 | μA | |
| I_{IL} | Low level input current | XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $V_I = 0 \text{ V}$ | | -4.0 | μA | |
| R_{PULLUP} | Pull-up resistor | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P17_4 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1) | $V_I = 0 \text{ V}$ | 50 | 100 | 500 | $\text{k}\Omega$ |
| R_{fXIN} | Feedback resistor | XIN | | 3 | | $\text{M}\Omega$ | |
| R_{fXCIN} | Feedback resistor | XCIN | | 25 | | $\text{M}\Omega$ | |

Note:

- Ports P16 to P19 are available in the 176-pin package only.

$$V_{CC} = 3.3 \text{ V}$$

Table 5.43 Electrical Characteristics (3/3)
($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit | |
|----------|---|---|---|------|---------------|------|---------------|
| | | | Min. | Typ. | Max. | | |
| I_{CC} | Power supply current | In single-chip mode, output pins are left open and others are connected to V_{SS} XIN-XOUT Drive power: low XCIN-XCOUT Drive power: low | $f_{(CPU)} = 64 \text{ MHz}$, $f_{(BCLK)} = 32 \text{ MHz}$, $f_{(XIN)} = 8 \text{ MHz}$, Active: XIN, PLL, Stopped: XCIN, OCO | | 40 | 55 | mA |
| | | | $f_{(CPU)} = f_{SO(PLL)}/24 \text{ MHz}$, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO | | 9 | | mA |
| | | | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256 \text{ MHz}$, $f_{(XIN)} = 8 \text{ MHz}$, Active: XIN, Stopped: PLL, XCIN, OCO | | 670 | | μA |
| | | | $f_{(CPU)} = f_{(BCLK)} = 32.768 \text{ kHz}$, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown | | 180 | | μA |
| | | | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4 \text{ kHz}$, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown | | 190 | | μA |
| | | | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256 \text{ MHz}$, $f_{(XIN)} = 8 \text{ MHz}$, Active: XIN, Stopped: PLL, XCIN, OCO, $T_a = 25^\circ\text{C}$, Wait mode | | 500 | 900 | μA |
| | | | $f_{(CPU)} = f_{(BCLK)} = 32.768 \text{ kHz}$, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, $T_a = 25^\circ\text{C}$, Wait mode | | 8 | 140 | μA |
| | | | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4 \text{ kHz}$, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, $T_a = 25^\circ\text{C}$, Wait mode | | 10 | 150 | μA |
| | Stopped: all clocks, Main regulator: shutdown, $T_a = 25^\circ\text{C}$ | | 5 | 70 | μA | | |

$$V_{CC} = 3.3 \text{ V}$$

Table 5.44 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 3.0$ to 3.6 V , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(BCLK)} = 32 \text{ MHz}$, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit | |
|---------------|--|---|--|------|-----------|---------------|-----|
| | | | Min. | Typ. | Max. | | |
| — | Resolution | $V_{REF} = V_{CC}$ | | | 10 | Bits | |
| — | Absolute error | $V_{REF} = V_{CC} = 3.3 \text{ V}$ | AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 | | | ±5 | LSB |
| | | | External op-amp connection mode | | | ±7 | LSB |
| INL | Integral non-linearity error | $V_{REF} = V_{CC} = 3.3 \text{ V}$ | AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 | | | ±5 | LSB |
| | | | External op-amp connection mode | | | ±7 | LSB |
| DNL | Differential non- linearity error | $V_{REF} = V_{CC} = 3.3 \text{ V}$ | | | ±1 | LSB | |
| — | Offset error | | | | ±3 | LSB | |
| — | Gain error | | | | ±3 | LSB | |
| R_{LADDER} | Resistor ladder | $V_{REF} = V_{CC}$ | 4 | | 20 | k Ω | |
| t_{CONV} | Conversion time (10 bits) | $\phi_{AD} = 10 \text{ MHz}$, with sample and hold function | 3.3 | | | μs | |
| t_{CONV} | Conversion time (8 bits) | $\phi_{AD} = 10 \text{ MHz}$, with sample and hold function | 2.8 | | | μs | |
| t_{SAMP} | Sampling time | $\phi_{AD} = 10 \text{ MHz}$ | 0.3 | | | μs | |
| V_{IA} | Analog input voltage | | 0 | | V_{REF} | V | |
| ϕ_{AD} | Operating clock frequency | without sample and hold function | 0.25 | | 10 | MHz | |
| | | with sample and hold function | 1 | | 10 | MHz | |
| $R_{PU(AST)}$ | Pull-up resistor for open-circuit detection | | 5 | 10 | 15 | k Ω | |
| $R_{PD(AST)}$ | Pull-down resistor for open-circuit detection | | 5 | 10 | 15 | k Ω | |

$$V_{CC} = 3.3 \text{ V}$$

Table 5.45 D/A Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 3.0$ to 3.6 V , $V_{SS} = AV_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

| Symbol | Characteristic | Measurement condition | Value | | | Unit |
|------------|-------------------------|-----------------------|-------|------|------|------------------|
| | | | Min. | Typ. | Max. | |
| — | Resolution | | | | 8 | Bits |
| — | Absolute precision | | | | 1.0 | % |
| t_s | Settling time | | | | 3 | μs |
| R_O | Output resistance | | 4 | 10 | 20 | $\text{k}\Omega$ |
| I_{VREF} | Reference input current | (1) | | | 1.0 | mA |

Note:

- One D/A converter is used. The DAi register ($i = 0, 1$) of the other unused converter is set to 00h. The resistor ladder for A/D converter is not considered.
Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.46 External Clock Input

| Symbol | Characteristic | Value | | Unit |
|-------------|---|-------|------|------|
| | | Min. | Max. | |
| $t_{C(X)}$ | External clock input period | 62.5 | 250 | ns |
| $t_{W(XH)}$ | External clock input high level pulse width | 25 | | ns |
| $t_{W(XL)}$ | External clock input low level pulse width | 25 | | ns |
| $t_{r(X)}$ | External clock input rise time | | 5 | ns |
| $t_{f(X)}$ | External clock input fall time | | 5 | ns |
| t_W / t_C | External clock input duty | 40 | 60 | % |

Table 5.47 External Bus Timing

| Symbol | Characteristic | Value | | Unit |
|----------------|------------------------------|-------|-------------------------------|------|
| | | Min. | Max. | |
| $t_{su(D-R)}$ | Data setup time for read | 40 | | ns |
| $t_{h(R-D)}$ | Data hold time after read | 0 | | ns |
| $t_{dis(R-D)}$ | Data disable time after read | | $0.5 \times t_{C(Base)} + 10$ | ns |

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.48 Timer A Input (Counting input in event counter mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input clock cycle time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN input high level pulse width | 80 | | ns |
| $t_{w(TAL)}$ | TAiIN input low level pulse width | 80 | | ns |

Table 5.49 Timer A Input (Gating input in timer mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input clock cycle time | 400 | | ns |
| $t_{w(TAH)}$ | TAiIN input high level pulse width | 180 | | ns |
| $t_{w(TAL)}$ | TAiIN input low level pulse width | 180 | | ns |

Table 5.50 Timer A Input (External trigger input in one-shot timer mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input clock cycle time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN input high level pulse width | 80 | | ns |
| $t_{w(TAL)}$ | TAiIN input low level pulse width | 80 | | ns |

Table 5.51 Timer A Input (External trigger input in pulse-width modulation mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN input high level pulse width | 80 | | ns |
| $t_{w(TAL)}$ | TAiIN input low level pulse width | 80 | | ns |

Table 5.52 Timer A Input (Increment/decrement count switching input in event counter mode)

| Symbol | Characteristic | Value | | Unit |
|------------------|-------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT input clock cycle time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT input high level pulse width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT input low level pulse width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT input setup time | 400 | | ns |
| $t_h(TIN-UP)$ | TAiOUT input hold time | 400 | | ns |

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.53 Timer B Input (Counting input in event counter mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|--|-------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input clock cycle time (one edge counting) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN input high level pulse width (one edge counting) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input low level pulse width (one edge counting) | 80 | | ns |
| $t_{c(TB)}$ | TBiIN input clock cycle time (both edges counting) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN input high level pulse width (both edges counting) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input low level pulse width (both edges counting) | 80 | | ns |

Table 5.54 Timer B Input (Pulse period measure mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input clock cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input high level pulse width | 180 | | ns |
| $t_{w(TBL)}$ | TBiIN input low level pulse width | 180 | | ns |

Table 5.55 Timer B Input (Pulse-width measure mode)

| Symbol | Characteristic | Value | | Unit |
|--------------|------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input clock cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input high level pulse width | 180 | | ns |
| $t_{w(TBL)}$ | TBiIN input low level pulse width | 180 | | ns |

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.56 Serial Interface

| Symbol | Characteristic | Value | | Unit |
|---------------|-----------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input clock cycle time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi input high level pulse width | 80 | | ns |
| $t_{w(CKL)}$ | CLKi input low level pulse width | 80 | | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 80 | | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | | ns |

Table 5.57 A/D Trigger Input

| Symbol | Characteristic | Value | | Unit |
|--------------|---|-----------------------|------|------|
| | | Min. | Max. | |
| $t_{w(ADH)}$ | ADTRG input high level pulse width Hardware trigger input high level pulse width | $\frac{3}{\phi_{AD}}$ | | ns |
| $t_{w(ADL)}$ | ADTRG input low level pulse width Hardware trigger input high level pulse width | 125 | | ns |

Table 5.58 External Interrupt INTi Input

| Symbol | Characteristic | | Value | | Unit |
|--------------|-----------------------------------|-----------------|--------------------|------|------|
| | | | Min. | Max. | |
| $t_{w(INH)}$ | INTi input high level pulse width | Edge sensitive | 250 | | ns |
| | | Level sensitive | $t_{c(CPU)} + 200$ | | ns |
| $t_{w(INL)}$ | INTi input low level pulse width | Edge sensitive | 250 | | ns |
| | | Level sensitive | $t_{c(CPU)} + 200$ | | ns |

Table 5.59 Intelligent I/O

| Symbol | Characteristic | Value | | Unit |
|----------------------|-------------------------------------|-------|------|------|
| | | Min. | Max. | |
| $t_{c(ISCLK2)}$ | ISCLK2 input clock cycle time | 600 | | ns |
| $t_{w(ISCLK2H)}$ | ISCLK2 input high level pulse width | 270 | | ns |
| $t_{w(ISCLK2L)}$ | ISCLK2 input low level pulse width | 270 | | ns |
| $t_{su(RXD-ISCLK2)}$ | ISRXD2 input setup time | 150 | | ns |
| $t_{h(ISCLK2-RXD)}$ | ISRXD2 input hold time | 100 | | ns |

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.60 Multi-master I²C-bus Interface

| Symbol | Characteristic | Value | | | | Unit |
|--------------------|---|---------------|------|---------------------------------|------|------|
| | | Standard-mode | | Fast-mode | | |
| | | Min. | Max. | Min. | Max. | |
| $t_{w(SCLH)}$ | MSCL input high level pulse width | 600 | | 600 | | ns |
| $t_{w(SCLL)}$ | MSCL input low level pulse width | 600 | | 600 | | ns |
| $t_{r(SCL)}$ | MSCL input rise time | | 1000 | | 300 | ns |
| $t_{f(SCL)}$ | MSCL input fall time | | 300 | | 300 | ns |
| $t_{r(SDA)}$ | MSDA input rise time | | 1000 | | 300 | ns |
| $t_{f(SDA)}$ | MSDA input fall time | | 300 | | 300 | ns |
| $t_{h(SDA-SCL)S}$ | MSCL high level hold time after start condition/restart condition | (1) | | $2 \times t_{c(\phi IIC)} + 40$ | | ns |
| $t_{su(SCL-SDA)P}$ | MSCL high level setup time for restart condition/stop condition | (1) | | $2 \times t_{c(\phi IIC)} + 40$ | | ns |
| $t_{w(SDAH)P}$ | MSDA high level pulse width after stop condition | (1) | | $4 \times t_{c(\phi IIC)} + 40$ | | ns |
| $t_{su(SDA-SCL)}$ | MSDA input setup time | 100 | | 100 | | ns |
| $t_{h(SCL-SDA)}$ | MSDA input hold time | 0 | | 0 | | ns |

Note:

- The value is calculated by the following formulas based on a value SSC set by bits SSC4 to SSC0 in the I2CSSCR register:

$$t_{h(SDA-SCL)S} = SSC \div 2 \times t_{c(\phi IIC)} + 40 \text{ [ns]}$$

$$t_{su(SCL-SDA)P} = (SSC \div 2 + 1) \times t_{c(\phi IIC)} + 40 \text{ [ns]}$$

$$t_{w(SDAH)P} = (SSC + 1) \times t_{c(\phi IIC)} + 40 \text{ [ns]}$$

$$V_{CC} = 3.3 \text{ V}$$

Switching Characteristics ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.61 External Bus Timing (Separate bus)

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|---------------|-----------------------------------|-----------------------|-------------------------------|------|------|
| | | | Min. | Max. | |
| $t_{su(S-R)}$ | Chip-select setup time for read | Refer to Figure 5.6 | (1) | | ns |
| $t_{h(R-S)}$ | Chip-select hold time after read | | $t_{c(Base)} - 15$ | | ns |
| $t_{su(A-R)}$ | Address setup time for read | | (1) | | ns |
| $t_{h(R-A)}$ | Address hold time after read | | $t_{c(Base)} - 15$ | | ns |
| $t_{w(R)}$ | Read pulse width | | (1) | | ns |
| $t_{su(S-W)}$ | Chip-select setup time for write | | (1) | | ns |
| $t_{h(W-S)}$ | Chip-select hold time after write | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{su(A-W)}$ | Address setup time for write | | (1) | | ns |
| $t_{h(W-A)}$ | Address hold time after write | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{w(W)}$ | Write pulse width | | (1) | | ns |
| $t_{su(D-W)}$ | Data setup time for write | | (1) | | ns |
| $t_{h(W-D)}$ | Data hold time after write | | 0 | | ns |

Note:

- The value is calculated by the following formulas based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_{w(R)}$, $T_{su(A-W)}$, and $T_{w(W)}$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For the details of how to set values, refer to the User's manual.

$$t_{su(S-R)} = t_{su(A-R)} = T_{su(A-R)} \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(R)} = T_{w(R)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$t_{su(S-W)} = t_{su(A-W)} = T_{su(A-W)} \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(W)} = t_{su(D-W)} = T_{w(W)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$V_{CC} = 3.3 \text{ V}$$

Switching Characteristics ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.62 External Bus Timing (Multiplexed bus)

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|-----------------|-----------------------------------|-----------------------|-------------------------------|------------------------|------|
| | | | Min. | Max. | |
| $t_{su(S-ALE)}$ | Chip-select setup time for ALE | Refer to Figure 5.6 | (1) | | ns |
| $t_{h(R-S)}$ | Chip-select hold time after read | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{su(A-ALE)}$ | Address setup time for ALE | | (1) | | ns |
| $t_{h(ALE-A)}$ | Address hold time after ALE | | $t_{c(Base)} - 5$ (2) | | ns |
| $t_{h(R-A)}$ | Address hold time after read | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{d(ALE-R)}$ | ALE-read delay time | | $t_{c(Base)} - 5$ (2) | $t_{c(Base)} + 10$ (2) | ns |
| $t_{W(ALE)}$ | ALE pulse width | | (1) | | ns |
| $t_{dis(R-A)}$ | Address disable time after read | | | 8 | ns |
| $t_{W(R)}$ | Read pulse width | | (1) | | ns |
| $t_{h(W-S)}$ | Chip-select hold time after write | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{h(W-A)}$ | Address hold time after write | | $1.5 \times t_{c(Base)} - 15$ | | ns |
| $t_{d(ALE-W)}$ | ALE-write delay time | | $t_{c(Base)} - 5$ (2) | $t_{c(Base)} + 10$ (2) | ns |
| $t_{W(W)}$ | Write pulse width | | (1) | | ns |
| $t_{su(D-W)}$ | Data setup time for write | | (1) | | ns |
| $t_{h(W-D)}$ | Data hold time after write | | $0.5 \times t_{c(Base)}$ | | ns |

Notes:

- The value is calculated by the following formulas based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_{W(R)}$, $T_{su(A-W)}$, and $T_{W(W)}$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For the details of how to set values, refer to the User's manual.

$$t_{su(S-ALE)} = t_{su(A-ALE)} = (T_{su(A-R)} - 1) \times t_{c(Base)} - 15 \text{ [ns]} \text{ (when } T_{su(A-R)} \text{ is greater than 1)}$$

$$t_{su(S-ALE)} = t_{su(A-ALE)} = 0.5 \times t_{c(Base)} - 15 \text{ [ns]} \text{ (when } T_{su(A-R)} \text{ is 1)}$$

$$t_{W(ALE)} = (T_{su(A-R)} - 1) \times t_{c(Base)} - 20 \text{ [ns]} \text{ (when } T_{su(A-R)} \text{ is greater than 1)}$$

$$t_{W(ALE)} = 0.5 \times t_{c(Base)} - 20 \text{ [ns]} \text{ (when } T_{su(A-R)} \text{ is 1)}$$

$$t_{W(R)} = T_{W(R)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$t_{W(W)} = t_{su(D-W)} = T_{W(W)} \times t_{c(Base)} - 10 \text{ [ns]}$$
- When $T_{su(A-R)}$ is greater than 1 or $T_{su(A-W)}$ is greater than 1. Change " $t_{c(Base)}$ " to " $0.5 \times t_{c(Base)}$ " when $T_{su(A-R)}$ is 1 or $T_{su(A-W)}$ is 1.

$$V_{CC} = 3.3 \text{ V}$$

Switching Characteristics ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.63 Serial Interface

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|--------------|------------------------|-----------------------|-------|------|------|
| | | | Min. | Max. | |
| $t_{d(C-Q)}$ | TXDi output delay time | Refer to Figure 5.6 | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi output hold time | | 0 | | ns |

Table 5.64 Intelligent I/O

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|-----------------|--------------------------|-----------------------|-------|------|------|
| | | | Min. | Max. | |
| $t_{d(ISTXD2)}$ | ISTXD2 output delay time | Refer to Figure 5.6 | | 180 | ns |
| $t_{h(ISTXD2)}$ | ISTXD2 output hold time | | 0 | | ns |

Table 5.65 Multi-master I²C-bus Interface (Standard-mode)

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|-------------------|--|-----------------------|-----------------------------------|-----------------------------------|------|
| | | | Min. | Max. | |
| $t_{f(SCL)}$ | MSCL output fall time | Refer to Figure 5.6 | 2 | | ns |
| $t_{f(SDA)}$ | MSDA output fall time | | 2 | | ns |
| $t_{d(SDA-SCL)S}$ | MSCL output delay time after start condition/restart condition | | $20 \times t_{c(\phi IIC)} - 120$ | $52 \times t_{c(\phi IIC)} - 40$ | ns |
| $t_{d(SCL-SDA)P}$ | Restart condition/stop condition output delay time after MSCL becomes high | | $20 \times t_{c(\phi IIC)} + 40$ | $52 \times t_{c(\phi IIC)} + 120$ | ns |
| $t_{d(SCL-SDA)}$ | MSDA output delay time | | $2 \times t_{c(\phi IIC)} + 40$ | $3 \times t_{c(\phi IIC)} + 120$ | ns |

Table 5.66 Multi-master I²C-bus Interface (Fast-mode)

| Symbol | Characteristic | Measurement condition | Value | | Unit |
|-------------------|--|-----------------------|-----------------------------------|-----------------------------------|------|
| | | | Min. | Max. | |
| $t_{f(SCL)}$ | MSCL output fall time | Refer to Figure 5.6 | 2 (1) | | ns |
| $t_{f(SDA)}$ | MSDA output fall time | | 2 (1) | | ns |
| $t_{d(SDA-SCL)S}$ | MSCL output delay time after start condition/restart condition | | $10 \times t_{c(\phi IIC)} - 120$ | $26 \times t_{c(\phi IIC)} - 40$ | ns |
| $t_{d(SCL-SDA)P}$ | Restart condition/stop condition output delay time after MSCL becomes high | | $10 \times t_{c(\phi IIC)} + 40$ | $26 \times t_{c(\phi IIC)} + 120$ | ns |
| $t_{d(SCL-SDA)}$ | MSDA output delay time | | $2 \times t_{c(\phi IIC)} + 40$ | $3 \times t_{c(\phi IIC)} + 120$ | ns |

Note:

- External circuits are required to satisfy the I²C-bus specification.

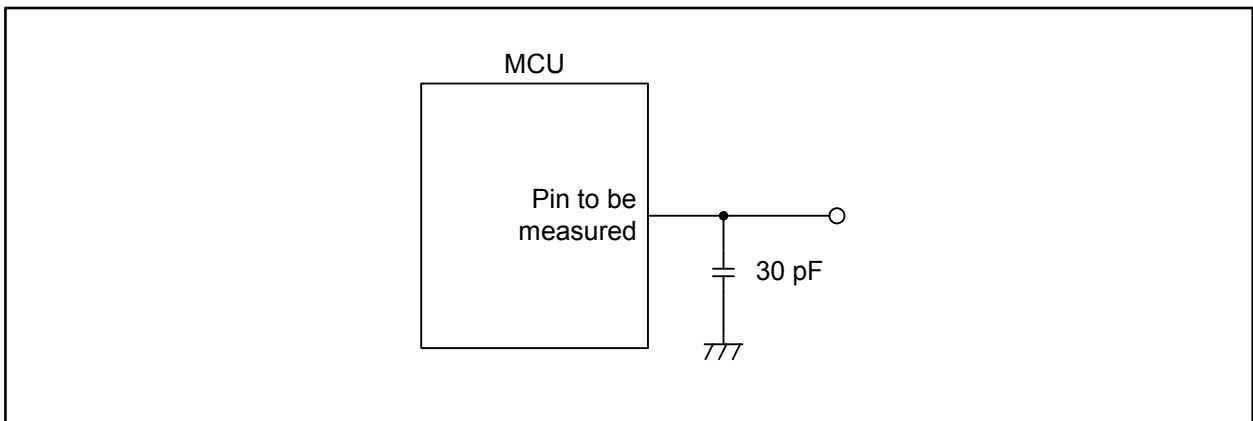


Figure 5.6 Switching Characteristic Measurement Circuit

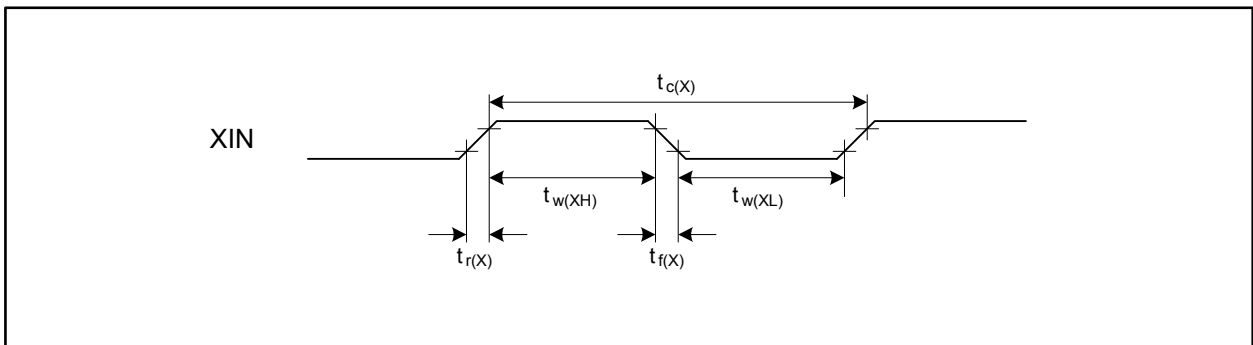


Figure 5.7 External Clock Input Timing

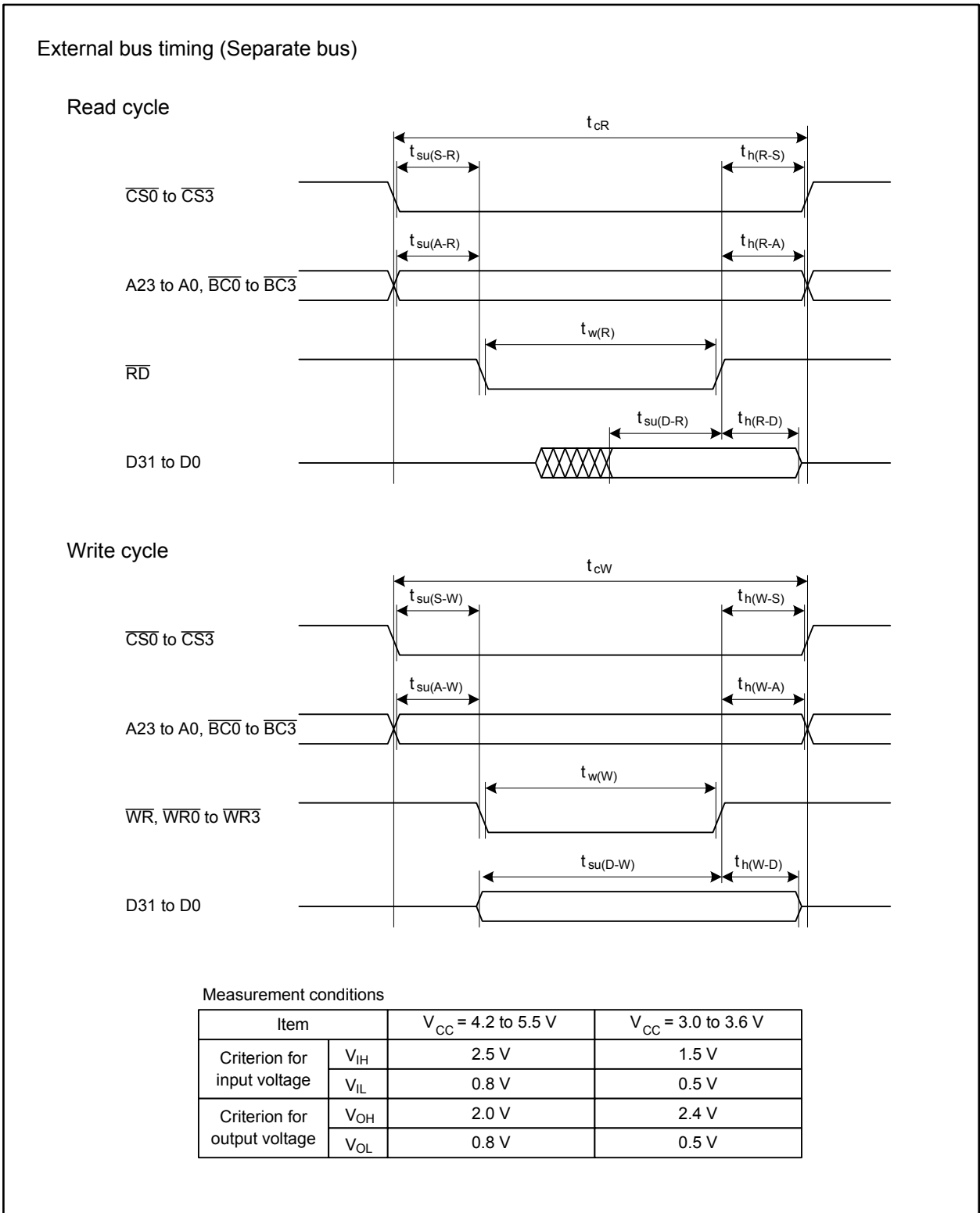


Figure 5.8 External Bus Timing (Separate Bus)

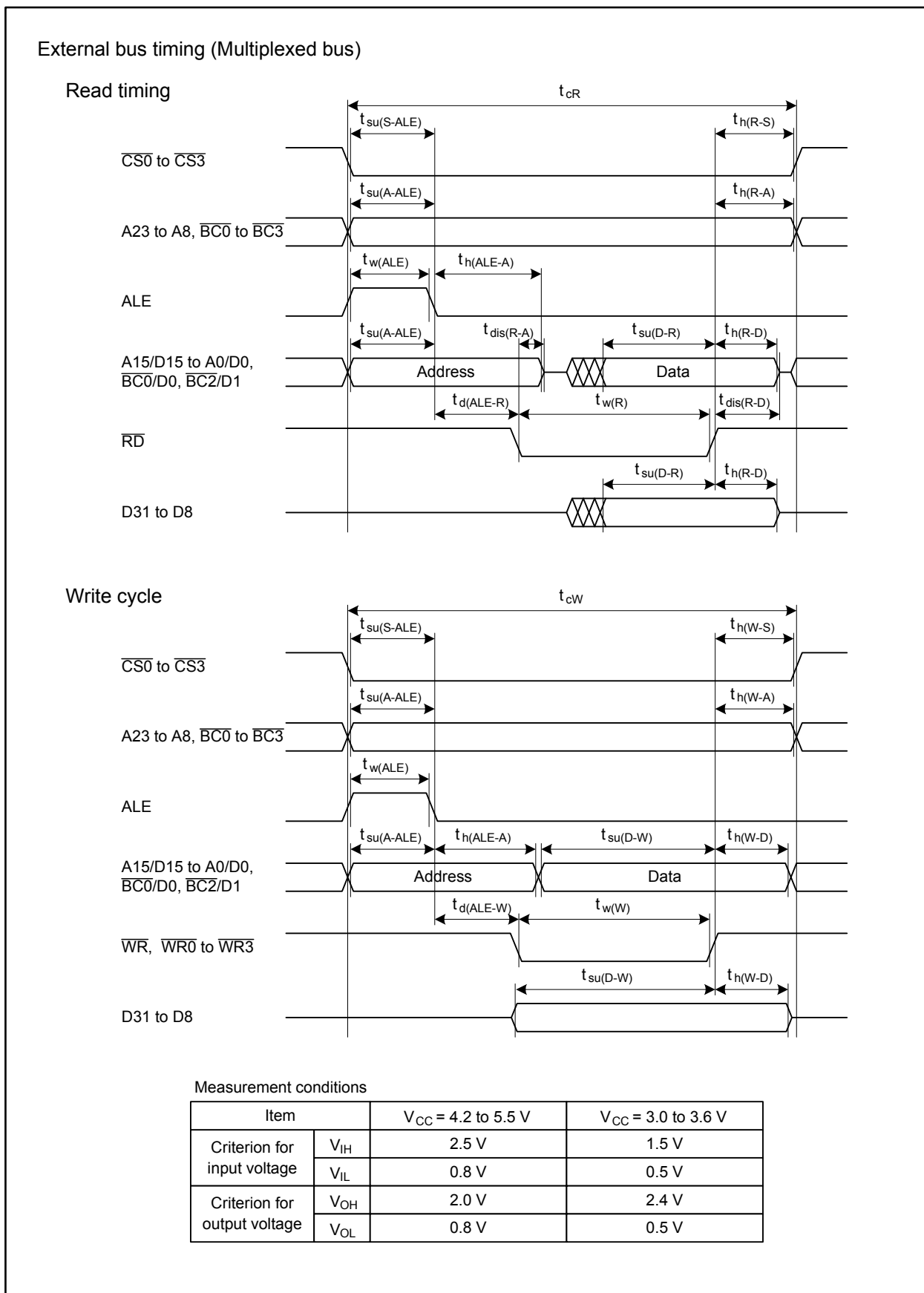


Figure 5.9 External Bus Timing (Multiplexed Bus)

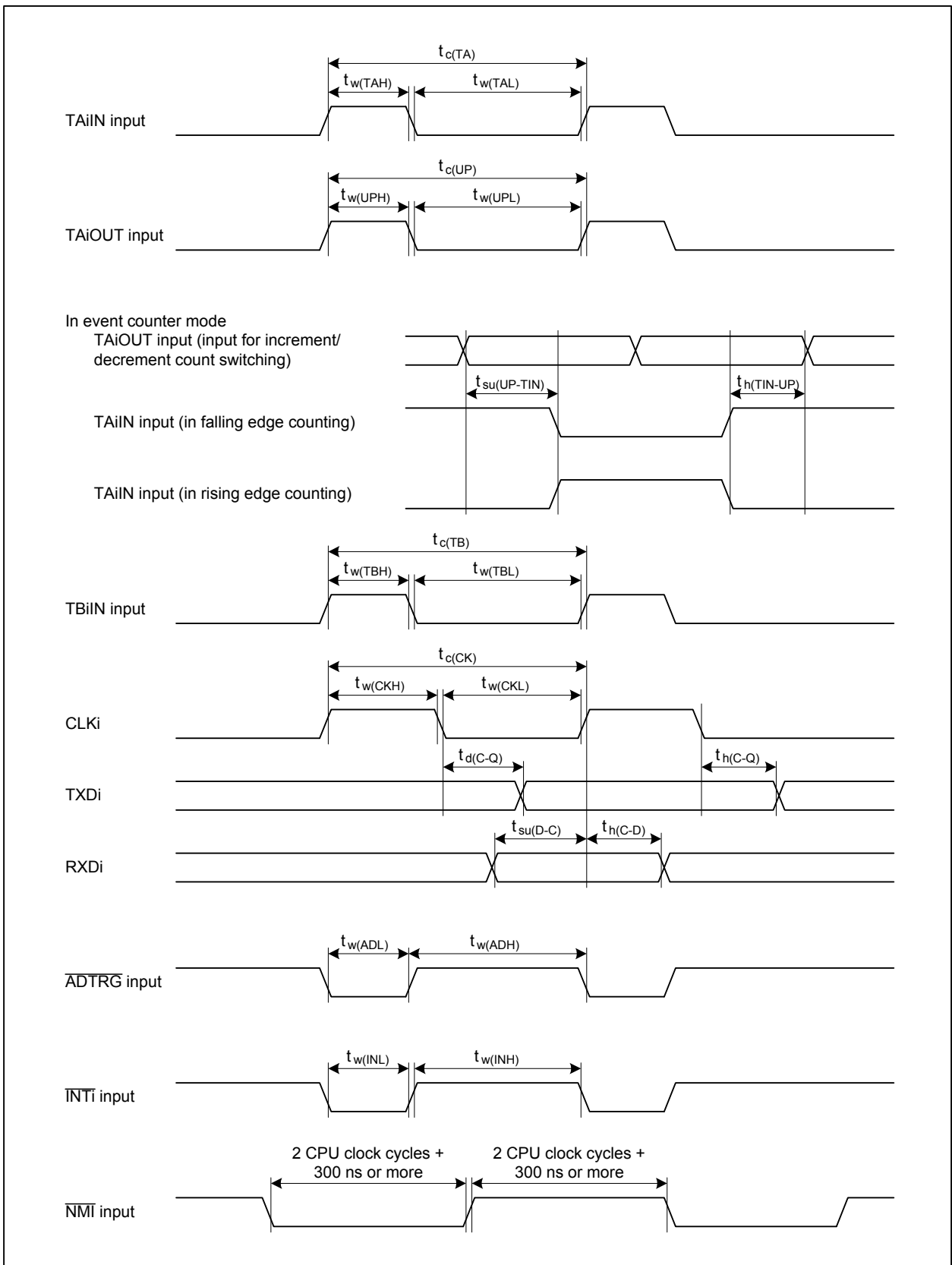


Figure 5.10 Timing of Peripheral Functions

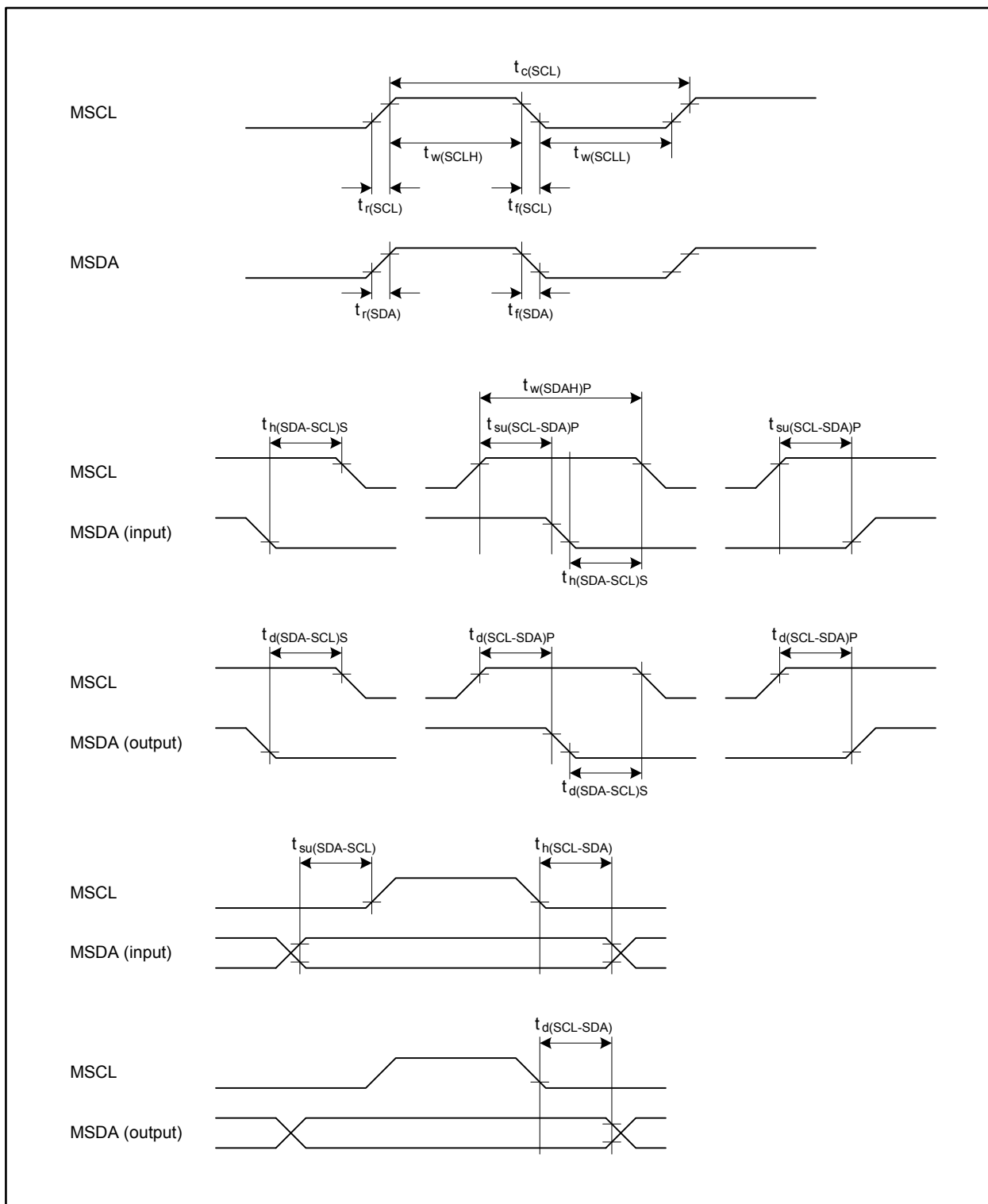
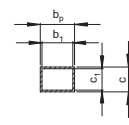
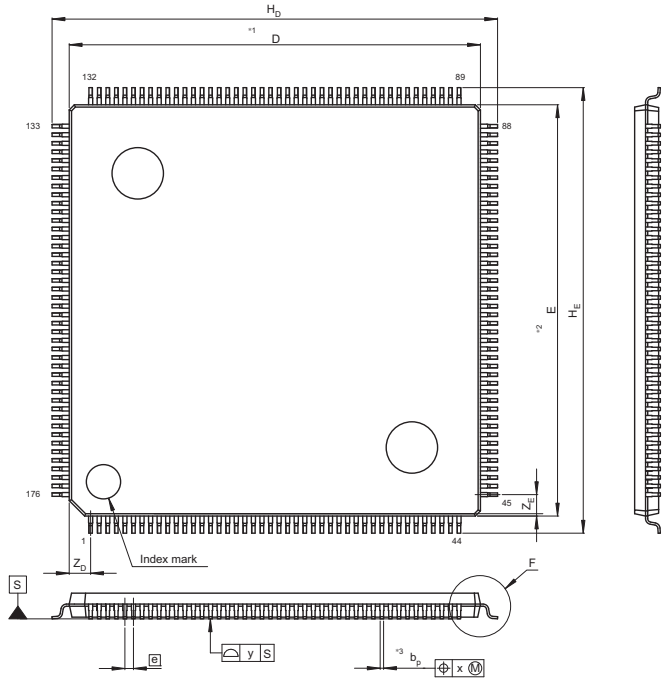


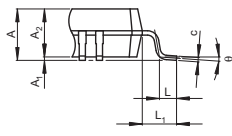
Figure 5.11 Timing of Multi-master I²C-bus Interface

Appendix 1. Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|----------------------|--------------|---------------------------|------------|
| P-LQFP176-24x24-0.50 | PLQP0176KB-A | 176P6Q-A/FP-176E/FP-176EV | 1.8g |



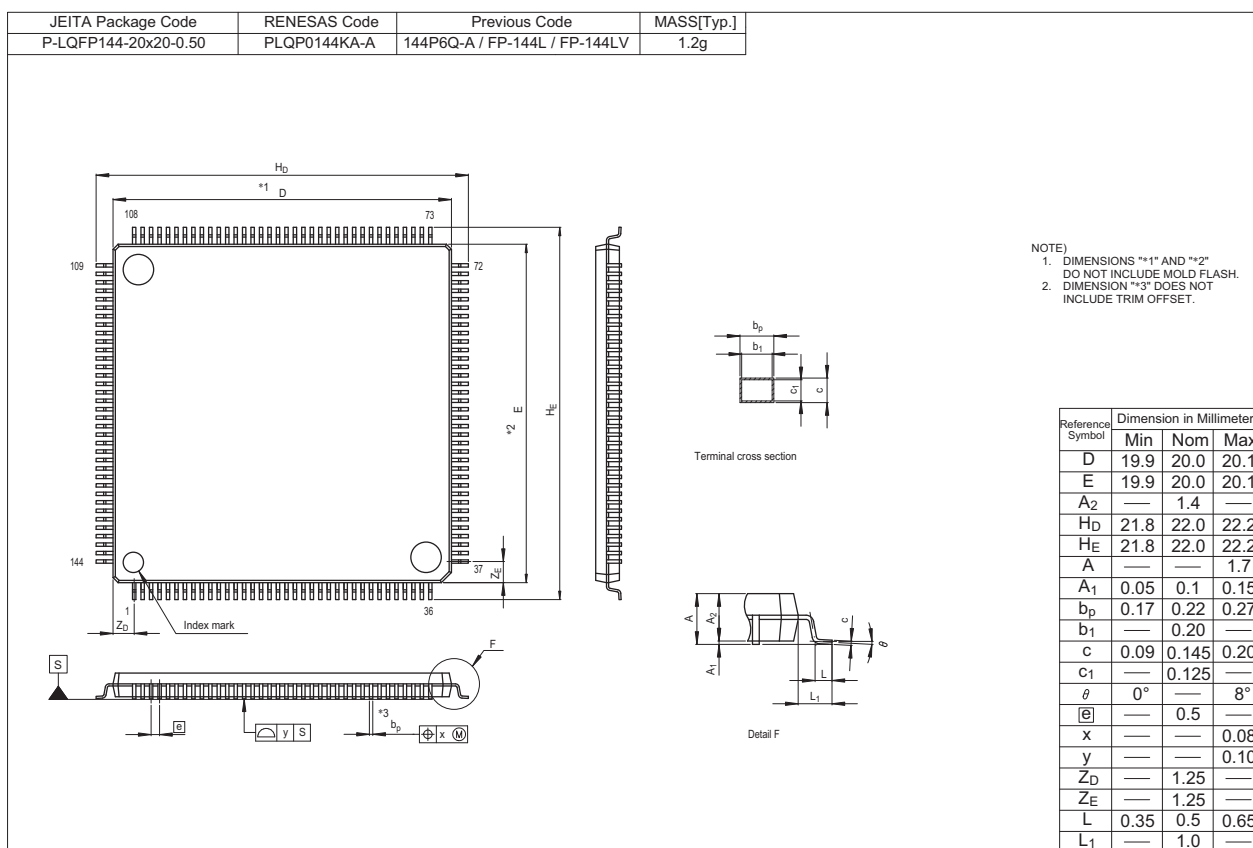
Terminal cross section



Detail F

NOTE)
 1. DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|------|
| | Min | Nom | Max |
| D | 23.9 | 24.0 | 24.1 |
| E | 23.9 | 24.0 | 24.1 |
| A ₂ | — | 1.4 | — |
| H _D | 25.8 | 26.0 | 26.2 |
| H _E | 25.8 | 26.0 | 26.2 |
| A | — | — | 1.7 |
| A ₁ | 0.05 | 0.1 | 0.15 |
| b _p | 0.15 | 0.20 | 0.25 |
| b ₁ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| c ₁ | — | 0.125 | — |
| θ | 0° | — | 8° |
| [e] | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| Z _D | — | 1.25 | — |
| Z _E | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| L ₁ | — | 1.0 | — |



| | |
|------------------|---------------------------|
| Revision History | R32C/118A Group Datasheet |
|------------------|---------------------------|

| Rev. | Date | Description | |
|------|--------------|--|---|
| | | Page | Summary |
| 0.50 | Mar 05, 2010 | — | Initial release |
| 1.00 | Jul 16, 2010 | — | Second edition released |
| | | — | <p>This manual in general</p> <ul style="list-style-type: none"> • Applied new Renesas templates and formats to the manual • Changed company name to “Renesas Electronics Corporation” and changed related descriptions due to business merger of Renesas Technology Corporation and NEC Electronics Corporation (under Chapters 1 and 5) • Modified expressions “version N”, “version D”, and “version P” to “N version”, “D version”, and “P version”, respectively (under Chapters 1 and 5) |
| | | 3, 5 6 8 20 | <p>Chapter 1. Overview</p> <ul style="list-style-type: none"> • Specified current consumptions in Tables 1.2 and 1.4; Deleted Note 1 • Corrected package codes in Table 1.5 • Deleted Note 1 from Figure 1.2 • Modified expression “fC” in Table 1.15 to “low speed clock” |
| | | 35, 38 40 42 44 55 70, 84 | <p>Chapter 4. SFRs</p> <ul style="list-style-type: none"> • Changed register name “Group i Timer Measurement Prescaler Register” in Tables 4.6 and 4.9 to “Group i Time Measurement Prescaler Register” • Modified expression “XY Control Register” in Table 4.11 to “X-Y Control Register” • Changed register name “UART2 Transmission/Receive Mode Register” in Table 4.13 to “UART2 Transmit/Receive Mode Register”; Changed hexadecimal format of reset values for registers TABSR, ONSF, and TRGSR to binary • Modified reset value “X00X X000b” for AD0CON2 register in Table 4.15 to “XX0X X000b” • Changed register name “External Interrupt Source Select Register i” in Table 4.26 to “External Interrupt Request Source Select Register i” • Modified register names “CANi Reception Error Count Register” and “CANi Transmission Error Count Register” in Tables 4.41 and 4.55 to “CANi Receive Error Count Register” and “CANi Transmit Error Count Register”, respectively |
| | | — | <p>Chapter 5. Electrical Characteristics</p> <ul style="list-style-type: none"> • Initially added |
| | | 126, 127 | <p>Appendix 1. Package Dimensions</p> <ul style="list-style-type: none"> • Added a seating plane to the drawing of package dimension |

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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